

Design Methodology toward DFM

STARCAD-21 overview

June 20, 2005

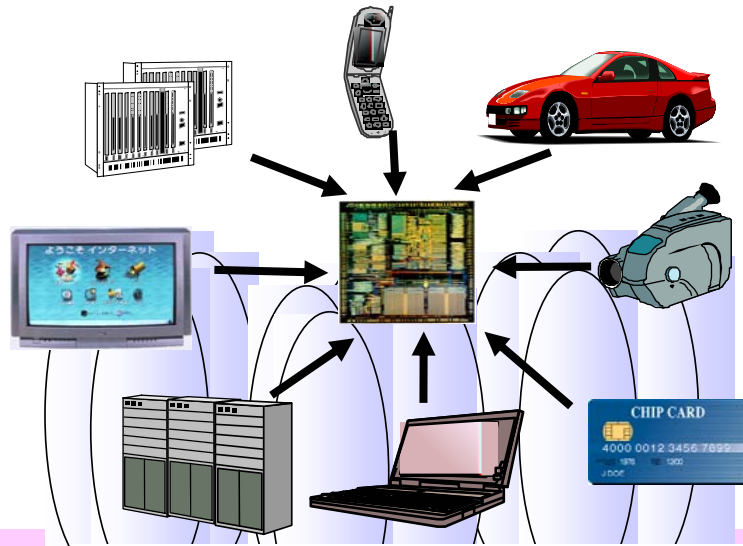
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Methodology Group, Development Department-1
STARC

This project is supported by Incorporated
Administrative Agency NEDO as a part
of the Focus 21 program

Industry Change in System LSI

Value up the design platform in System LSI as industry standard



Market oriented design platform

**Standard design platform
(Design Methodology)**

*Integrating Japanese engineering know-how
Leading related vendors*

Marketing and new products
in order to create new markets



Enterprise

**Focusing on differentiating
market segment**

Difficulties in design due to
nanometer technology and
huge development cost for design
system



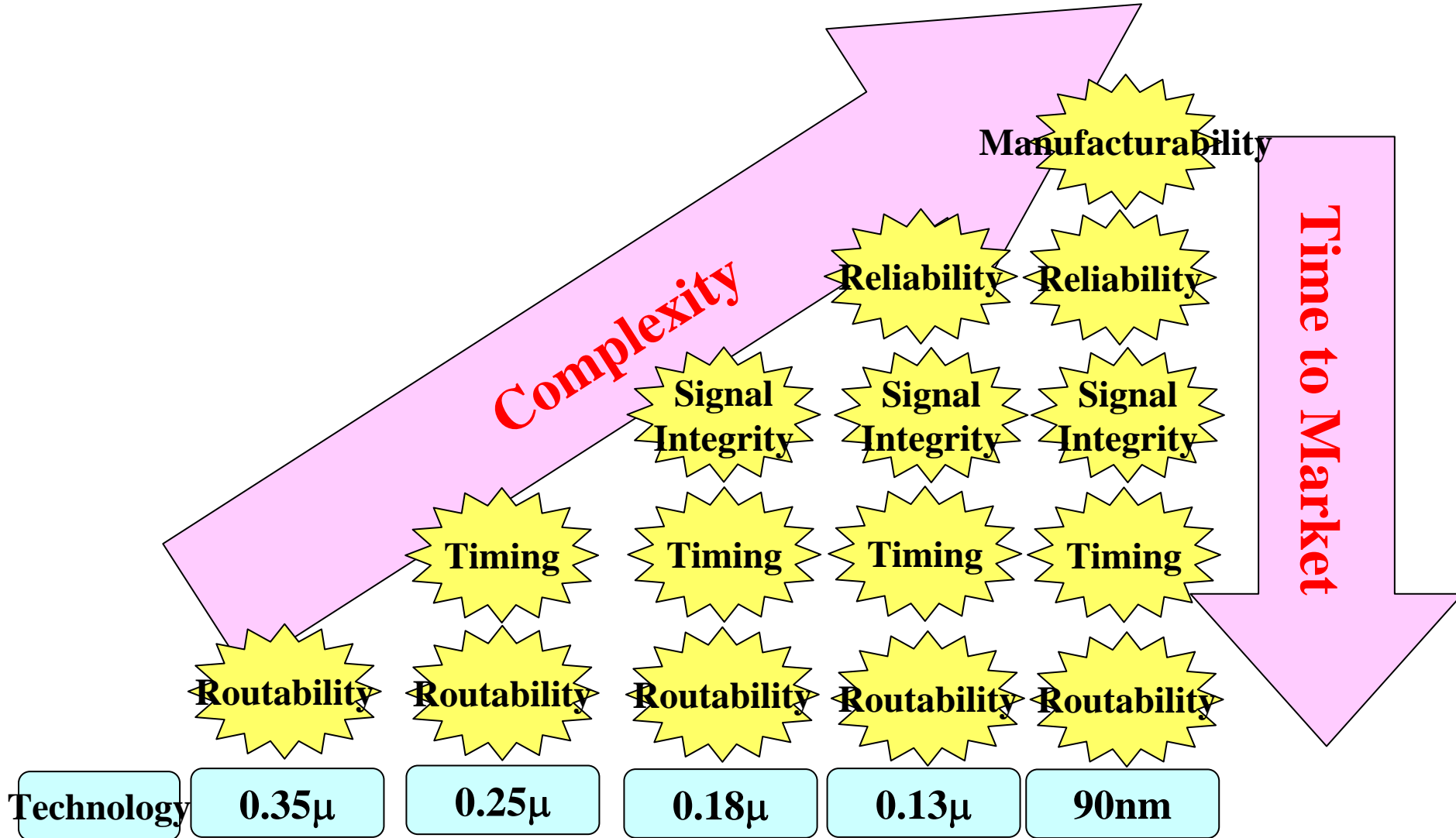
Consortium



Industry Standard

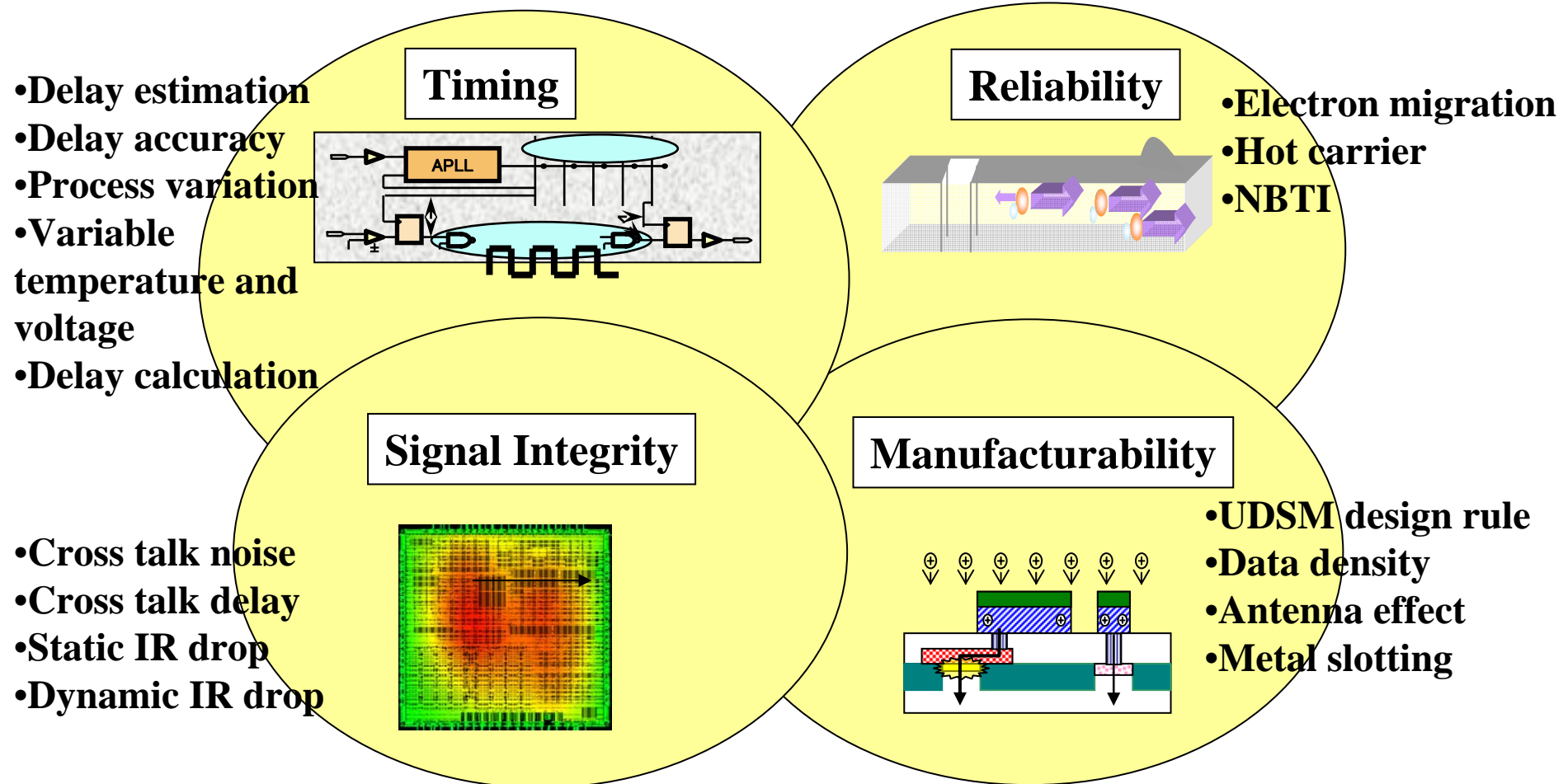


Design Complexity



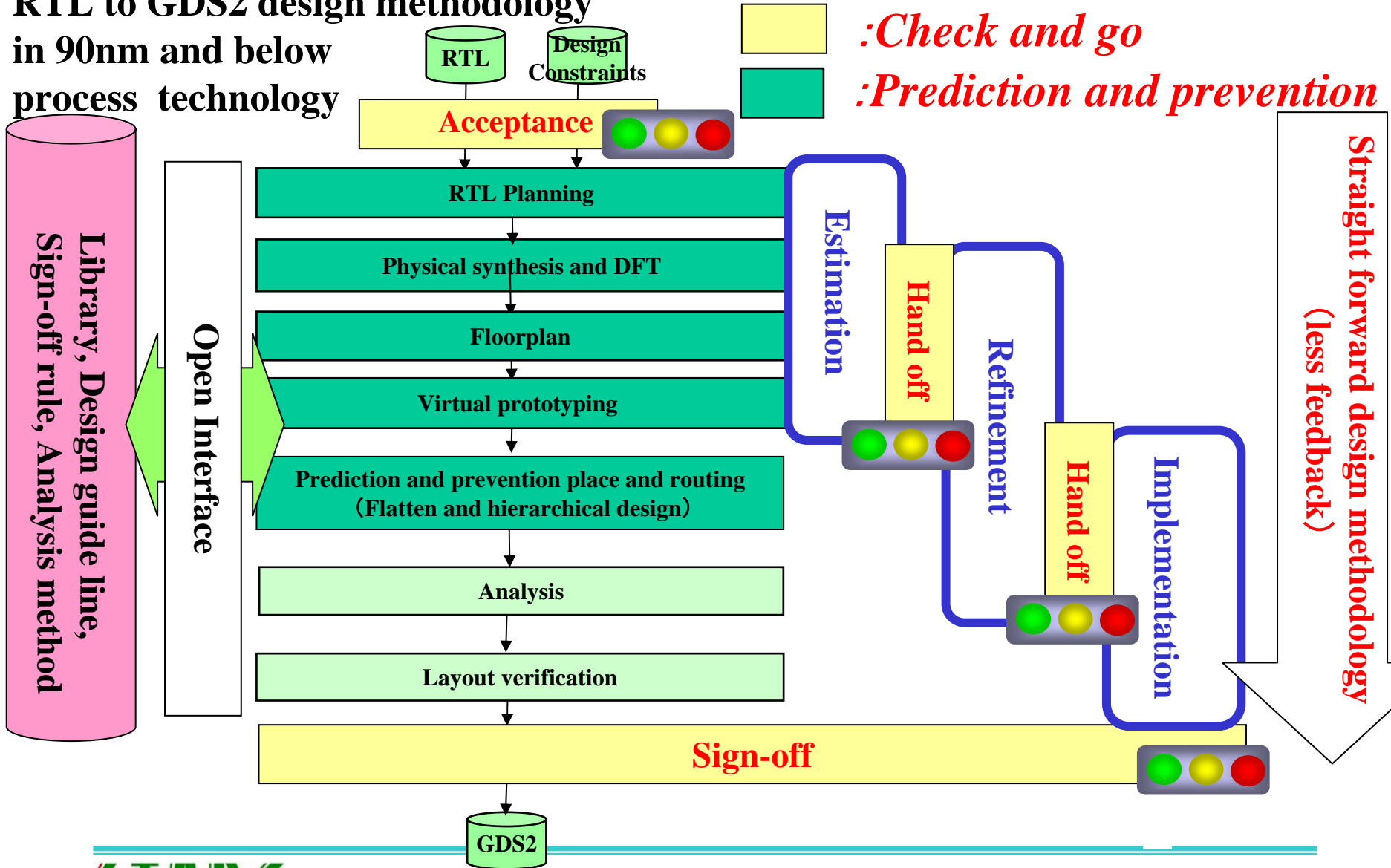
Key issues in UDSM phenomena

Timing, Signal Integrity, Reliability and Manufacturability
are **NOT independent** but **trade off**



Design methodology for production

RTL to GDS2 design methodology
in 90nm and below
process technology



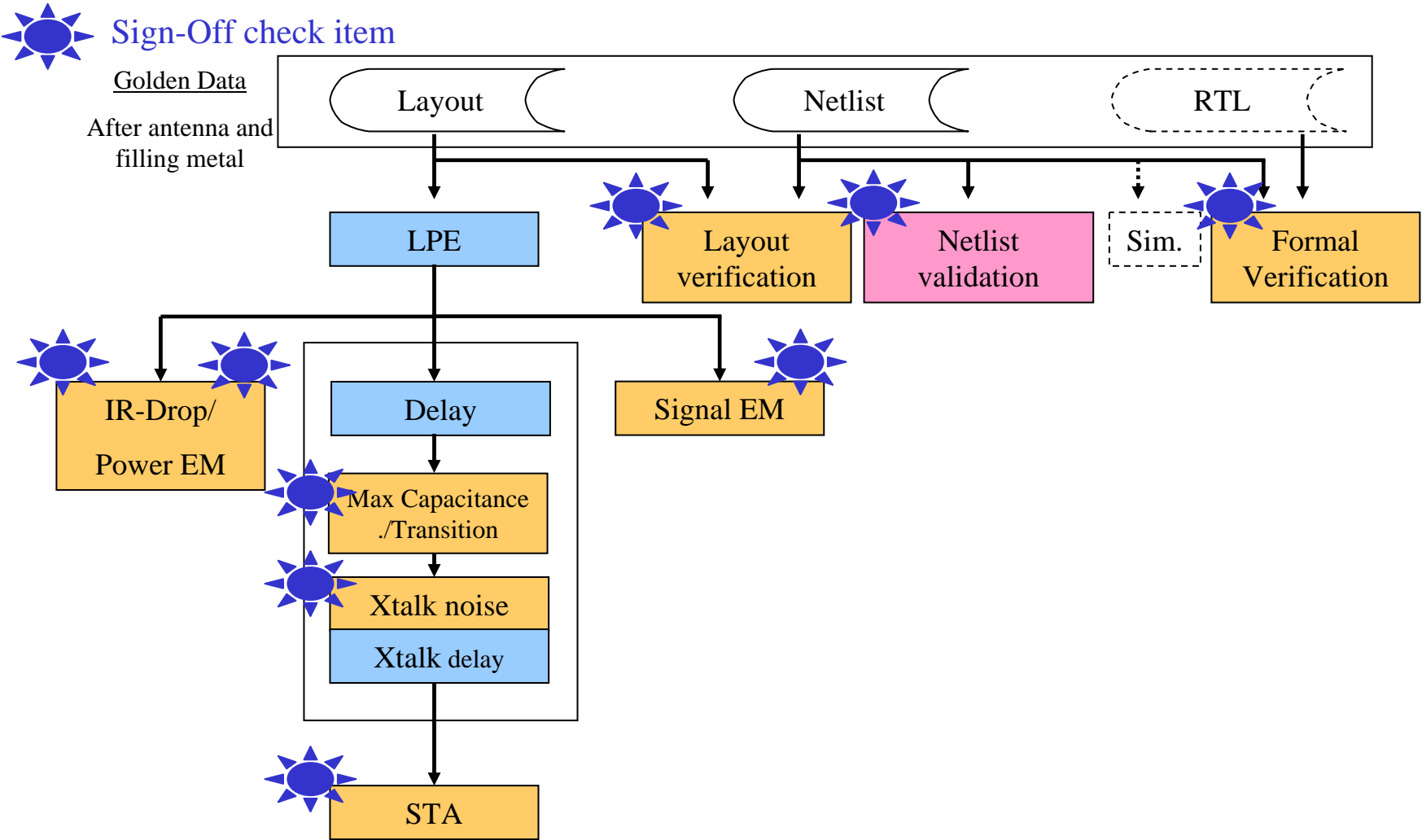
Main release schedule

- Basic design methodology
 - RTLtoGDS2 basic design flow (V1.0 2004/4)
- Standard design methodology
 - Huge design solution (Hierarchical, Flat) (V1.5 2004/10)
 - Low power design solution (V2.0 2005/4)
- High effective design methodology (V2.5 2005/10, V3.0 2006/3)
 - Reduction of design turn around time
 - Reduction of design margin

Features in V1.0

- Basic design methodology in 90nm technology
 - Design tool chain based on commercial EDA products
 - Integrated methodology for timing, SI and DFM closures
 - Higher efficiency in timing with pseudo hierarchical design
 - New design database recommended by EDA vendor
- Consistent EDA library specification with EDA tool
 - Focusing on timing and SI
- Clear sign-off rule taken into account of process variation
 - Consideration of process variation without any penalty in timing closure
- Important tool evaluation for 90nm phenomena analysis
 - Focusing on CTS, SI, LPE and EM

Sign-off check flow



Inserting double via as DFM

The screenshot displays the Cadence Encounter PCB design environment. The main workspace shows a complex routing layout with various colored traces and vias. The interface includes a menu bar at the top with options like Design, FlipChip, Partition, Floorplan, Place, Clock, Route, Timing, SI, Power, Verify, and Tools. A toolbar is located below the menu bar. On the left side, there is a vertical toolbar with icons for various design tools, and a panel for Explorer and Views. On the right side, there is a color legend titled "All Colors" with a table of color swatches for different design elements. Below the legend, there are logos for STARC and cadence, and a list of design rules: ZD flow, Phase 1, Phase 2, and Phase 3. The status bar at the bottom shows the coordinates (685.155, 642.490).

| Category | Color |
|-----------|--------------|
| Module | Light Green |
| Black Box | Dark Green |
| Fence | Orange |
| Guide | Pink |
| Obstruct | Red |
| Region | Light Blue |
| Screen | Light Yellow |
| Instance | Cyan |
| Net | Blue |
| SNet | Light Yellow |
| Pin | White |
| Ruler | Yellow |
| VCongest | Dark Blue |
| HCongest | Dark Blue |
| Text | White |

STARC
EDS Fair 2004
cadence

ZD flow
Phase 1
Phase 2
Phase 3

(685.155, 642.490)

Inserting dummy metal as DFM

The screenshot displays the Cadence Encounter PCB design environment. The main workspace shows a routed PCB layout with a grid and various design rules. The top menu bar includes Design, Flip Chip, Partition, Floorplan, Place, Clock, Route, Timing, SI, Power, Verify, and Tools. The status bar indicates the design is Routed.

On the left side, there is a Tools palette with various icons for design operations. Below it is an Explorer pane showing system icons like Hummingbird, Microsoft Outlook, and Adobe Reader. At the bottom left, a terminal window shows the following text:

```
kterm
Begin :
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Begin :
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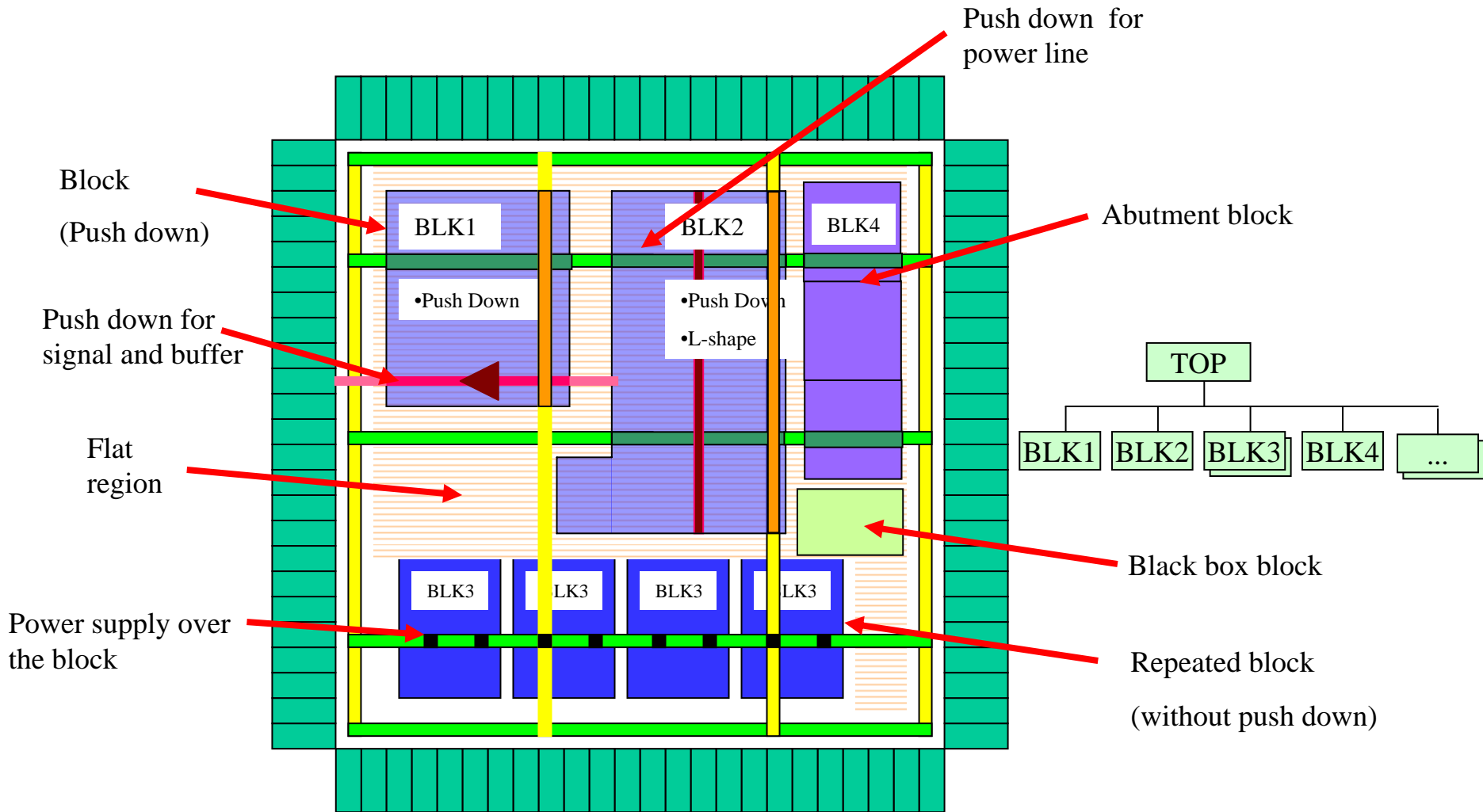
On the right side, there is a color legend titled "All Colors" with a table of colors and their corresponding design elements:

| Color | V | S |
|-----------|---|---|
| Module | | |
| Black Box | | |
| Fence | | |
| Guide | | |
| Obstruct | | |
| Region | | |
| Screen | | |
| Instance | | |
| Net | | |
| SNet | | |
| Pin | | |
| Ruler | | |
| VCongest | | |
| HCongest | | |
| Text | | |

Below the color legend, there is a STARC logo and the text "EDS Fair 2004 cadence". At the bottom right, there are three buttons labeled "ZD flow", "Phase 1", "Phase 2", and "Phase 3".



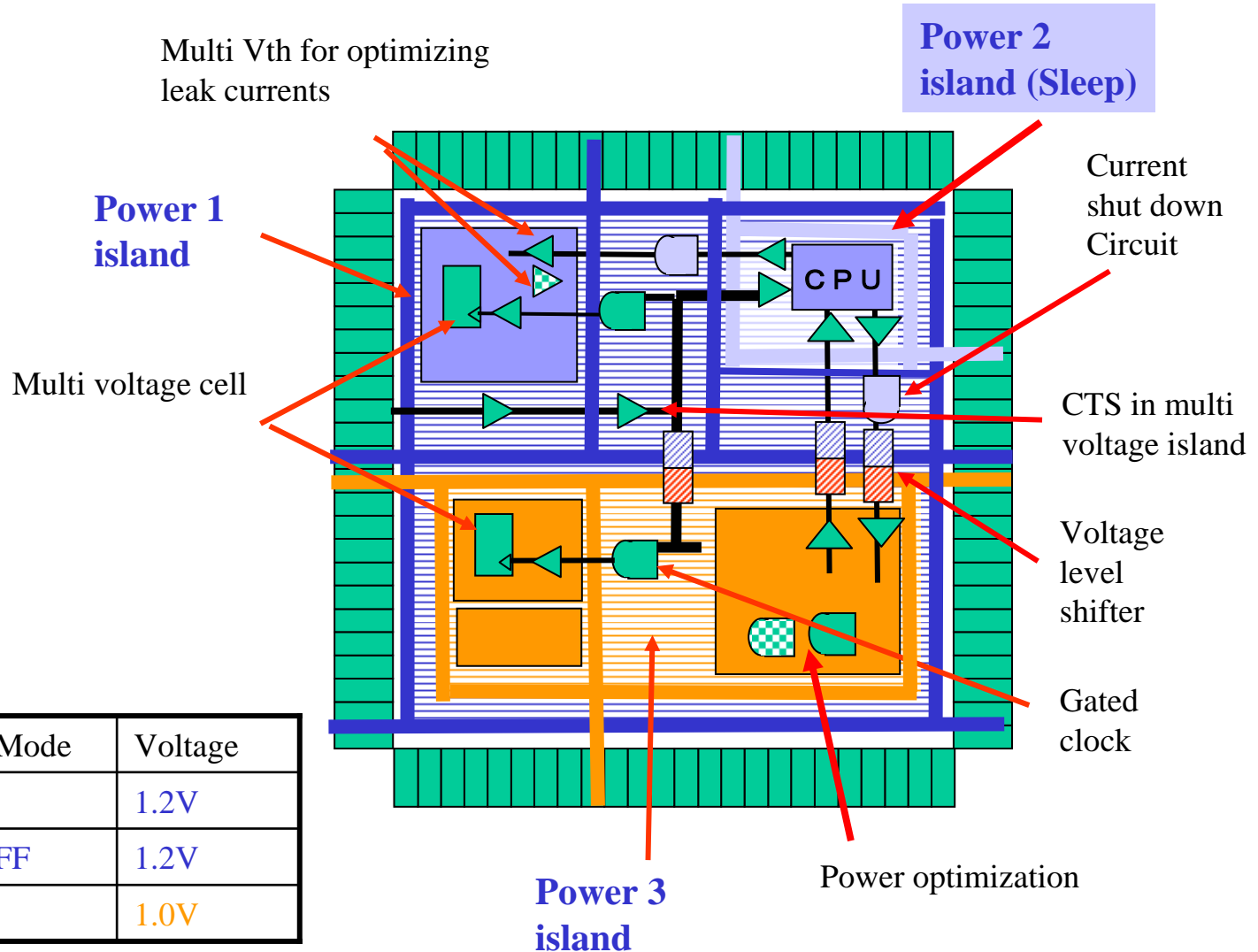
V1.5 Hierarchical design - Chip image -



Features in V1.5

- Hierarchical design methodology to take true benefit
- Reduction for timing verification corners
- Definition for verification corners in cross talk noise, IR drop and signal EM
- SDC checker
- IP modeling specification in hierarchical design

V2.0 Low power design - Chip image -



Features in V2.0

- Low power design
 - Design flow for multi power with power shut down operation
 - Design flow for multi Vth
 - Design rule check for multi power
(Ex. Power island, Level shifter insertion)
 - Cross talk analysis in multi power (among different powers)
 - Multi power supply voltage libraries
 - 1.2V and 1.0V
 - Delay calculation and noise analysis
 - Gated clock with cloning and decloning
 - CTS in multi power

Features in V2.0

- V variable library in each supply voltage (Single library and accurate interpolate tool)
- Considerations of IR drop at each instance
- Power analysis with switching toggle
- Power line noise analysis
- Effective max capacitance and max transition constraints handling
- Integration with SDC checker and SDC generator
- Reduction in pessimistic cross talk noise by noise immunity
- Avoidance in signal EM
- Enhancement in inserting dummy metal with less impact in timing and SI

Multi voltage libraries

■ Specification of multi voltage

| | Voltage [v] | | | Temperature [°C] |
|--------------|-------------|-----------|---------|------------------|
| | base | variation | IR-Drop | |
| High Voltage | 1.2 | ±0.1 | - 0.1 | - 40~125 |
| Low Voltage | 1.0 | ±0.05 | - 0.1 | - 40~125 |

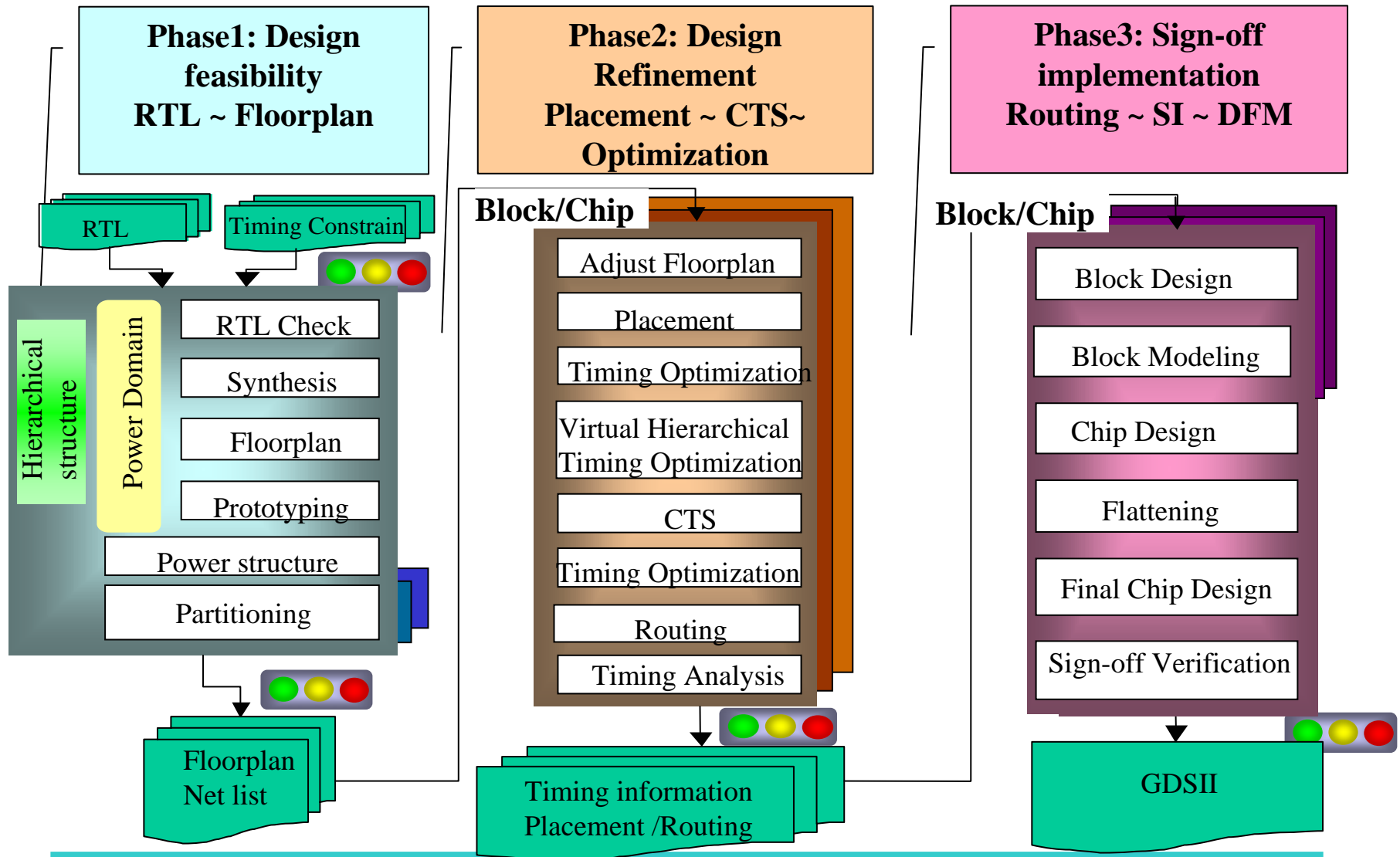
■ Characterize conditions

| | Process | MAX(SS) | | TYP(TT) | MIN(FF) | |
|-------------|----------------|---------|-------|---------|---------|-------|
| | Temp. | -40 | 125 | 25 | -40 | 125 |
| H-Vdd(1.2v) | | 1.1V | 1.1V | 1.2V | 1.3V | 1.3V |
| | IR-Drop(-0.1v) | 1.0V | 1.0V | | 1.2V | 1.2V |
| L-Vdd(1.0v) | | 0.95V | 0.95V | 1.0V | 1.05V | 1.05V |
| | IR-Drop(-0.1v) | 0.85V | 0.85V | | 0.95V | 0.95V |

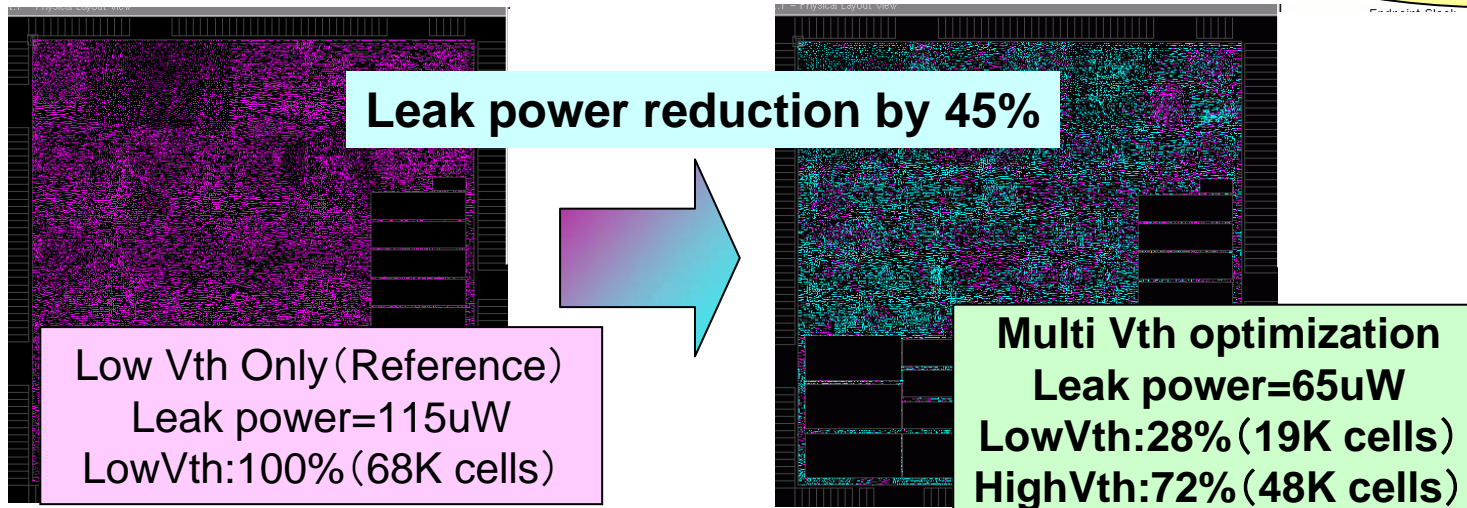
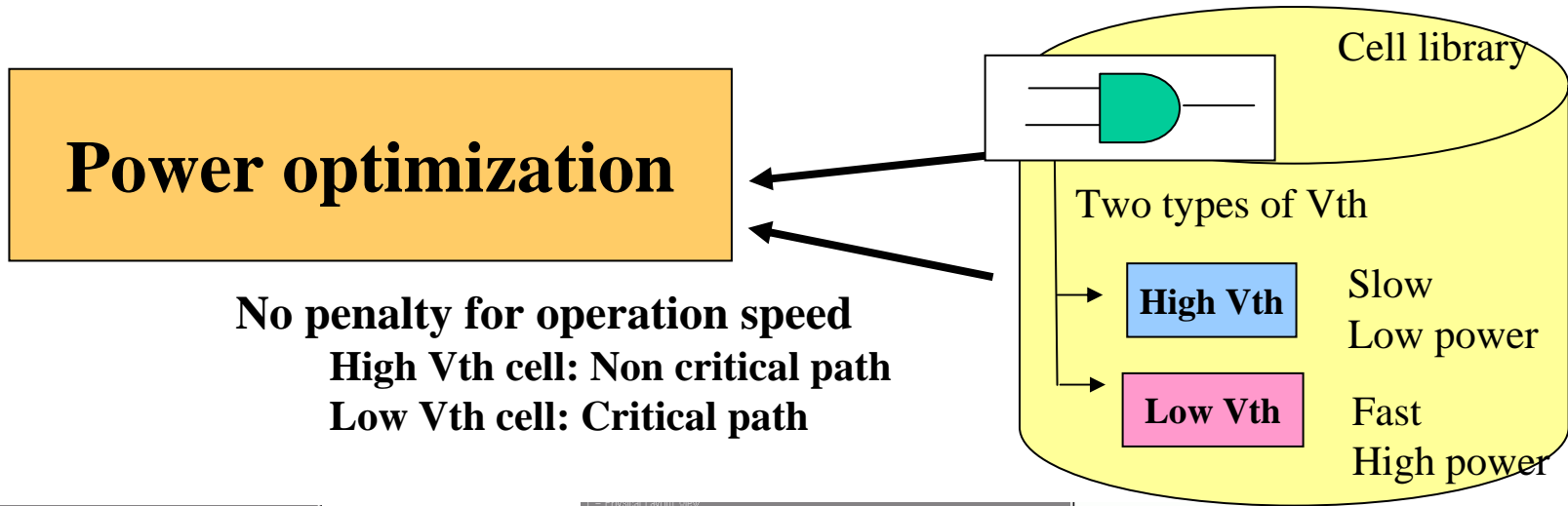
| | Process | MAX(SS) | | TYP(TT) | MIN(FF) | |
|-----|---------|---------|------|---------|---------|------|
| | Temp. | -40 | 125 | 25 | -40 | 125 |
| I/O | | 1.1V | 1.1V | 1.2V | 1.3V | 1.3V |

| | Process | MAX(SS) | | TYP(TT) | MIN(FF) | |
|---------------|---------|------------|------------|-----------|------------|------------|
| | Temp. | -40 | 125 | 25 | -40 | 125 |
| Level shifter | | 1.1V | 1.1V | 1.2V | 1.3V | 1.3V |
| | | ↓ 0.95V | ↓ 0.95V | ↓ 1.0V | ↓ 1.05V | ↓ 1.05V |

Production flow for low power design



Power reduction by selecting Multi-Vth



Effectiveness in low power design

Reducing power to
50% at the shutting down mode
40% at the active mode

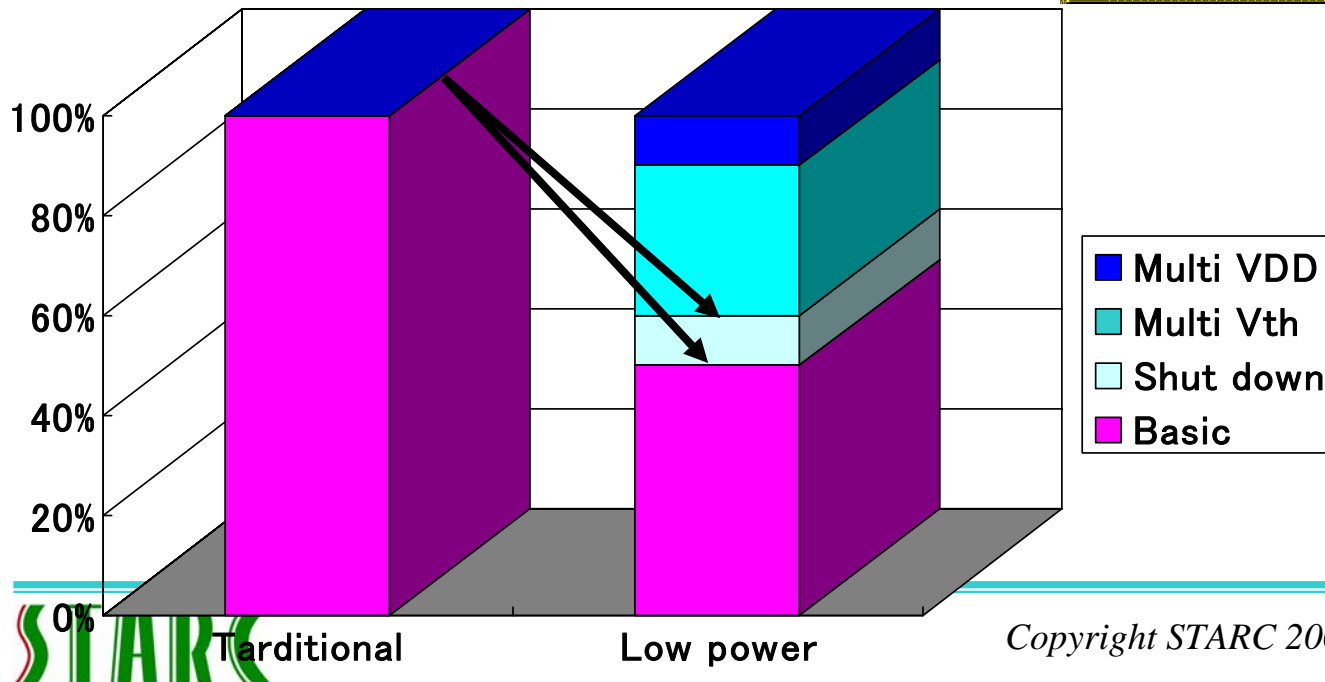
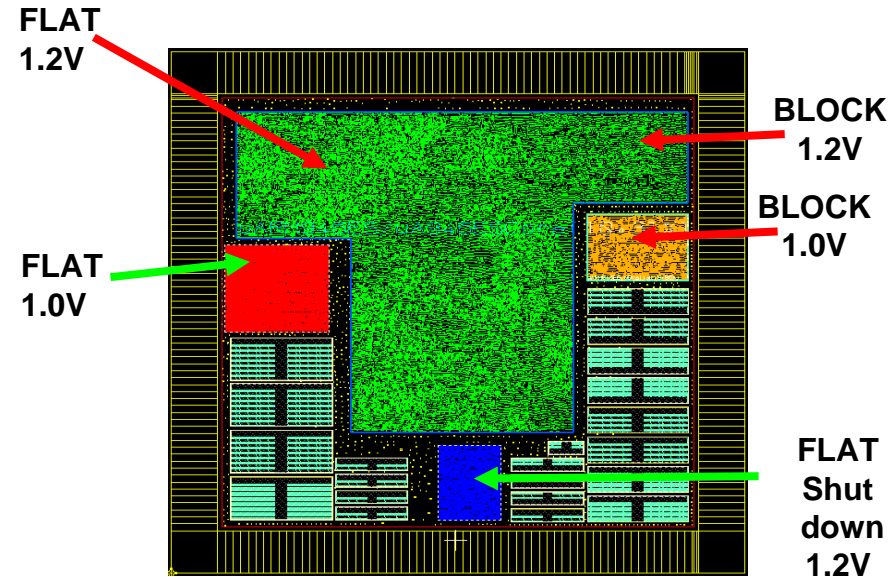
System LSI (example)

1.2V area (Active) : 70%

- Useable high V_{th} cell

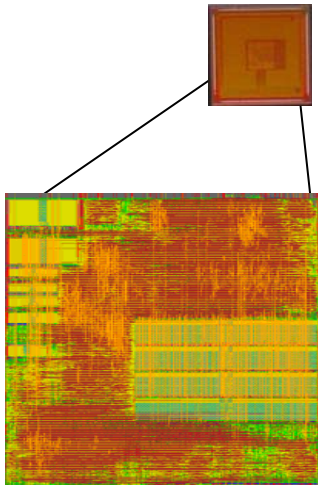
1.2V area (with power shut down) : 10%

1.0V area : 20%

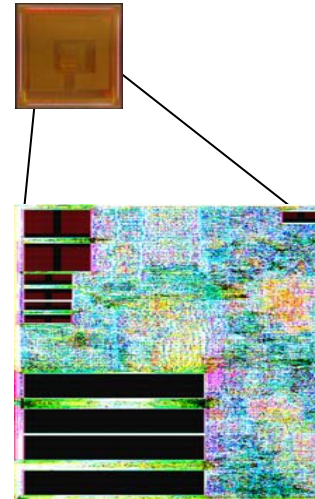


First silicon success!!

Methodology verification project(SH-4)



ZD flow



Pegasus flow

By using the STARCAD-21 which is fully integrated design methodology

- Grant a chip to work in production on the computer environment at design phase (Sign-off)
- Realize similar design turn around time in 90nm to 130nm (33% up in productivity)
- Complete solution in 90nm technology difficulty such as timing, signal integrity and design for manufacturing

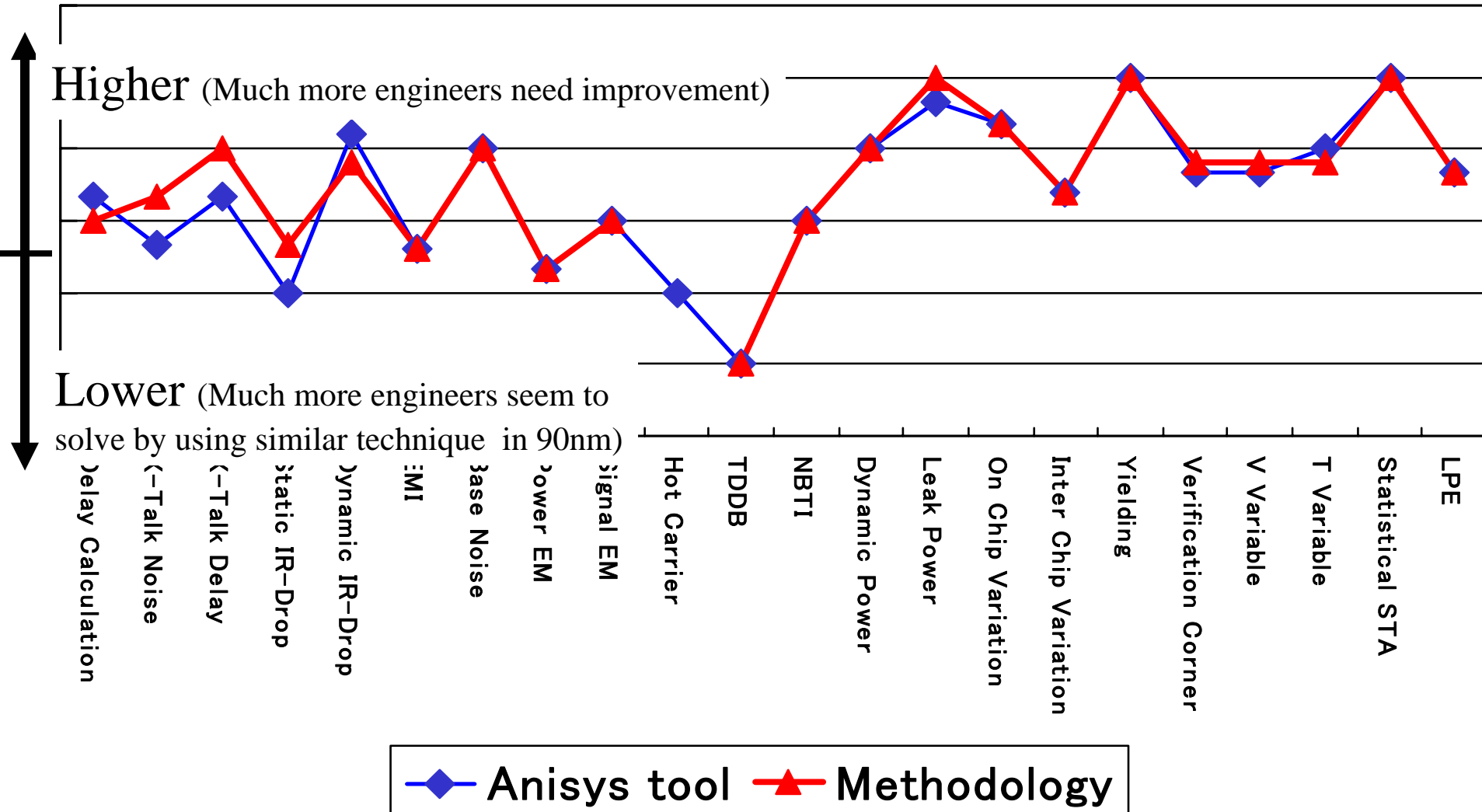
De-facto standard in SOC design methodology

Beyond V2.0

- Reducing design turn around time drastically
 - Enhance for timing constraints handling
 - Multi corners, Multi scenario
 - Golden timing constraint flow
 - Reducing sign-off corners
 - Timing and SI
 - Good hand-off criteria
 - Hierarchical sign-off
- Less design margin
 - On-chip variation
 - Considerations instance base IR-drop more effectively
 - Tool accuracies
- 65nm design methodology with DFM

Importance for DFM design factor in 65nm

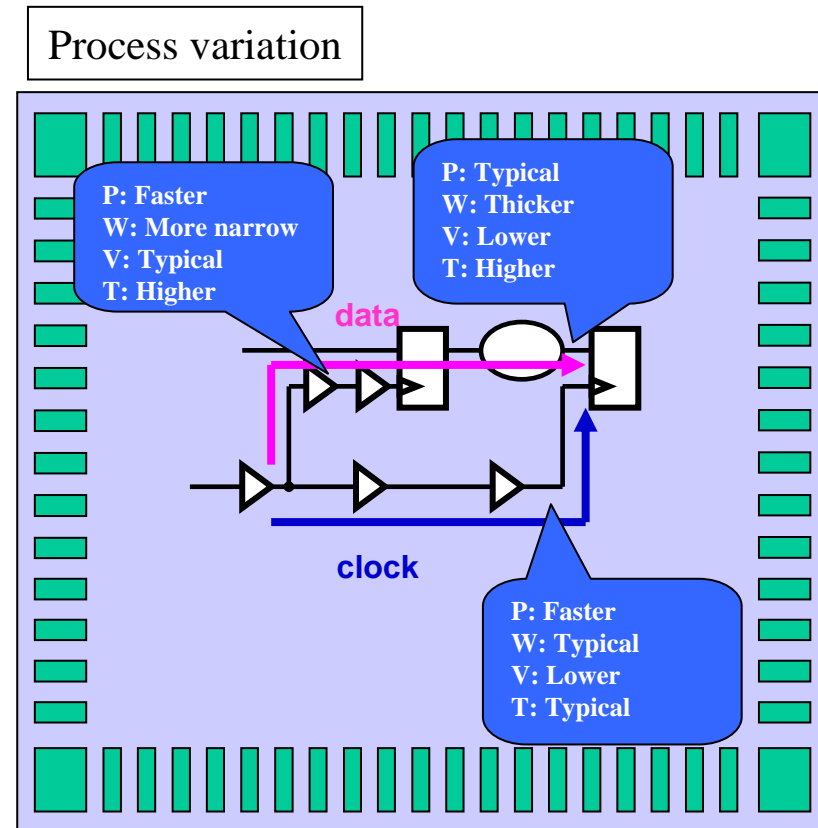
Comparing with 90nm



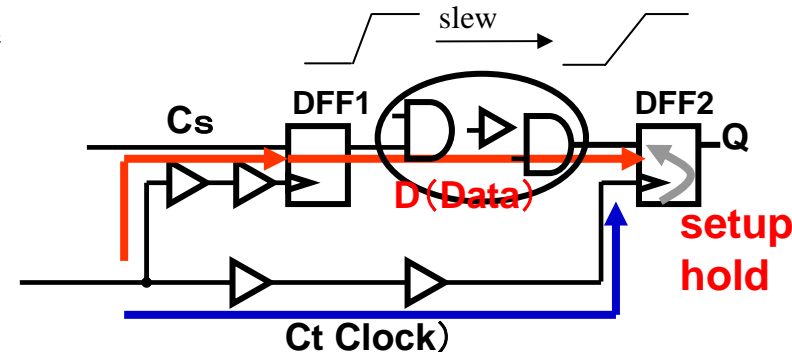
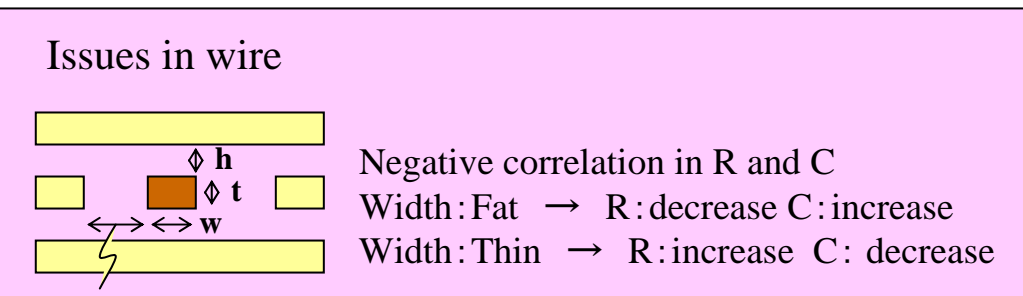
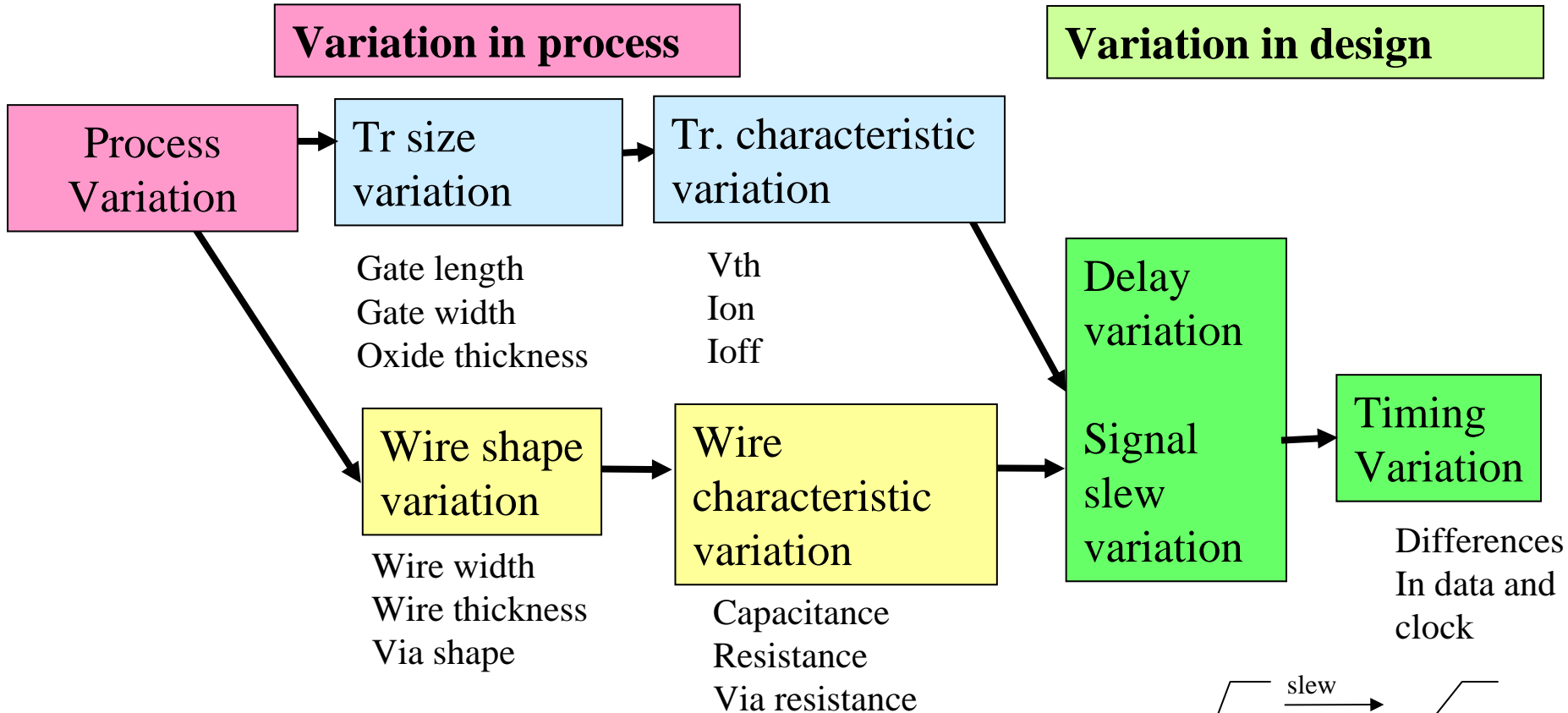
Verification with OCV (On-Chip-Variation)

- What is OCV?
 - **Process variation**
 - Incompleteness on OPC (Optical Proximity Correction)
 - Hard consideration in design
 - Temperature in chip
 - Instance base IR drop
 - Other design margins
 - Tool accuracy
- Current verification
 - Verification corner
In order to guarantee chip operation several different sets in
 - P: Process (Transistor process)
 - W: Wire (Wire process)
 - V: Voltage (Supply voltage) and
 - T: Temperature
 - Verifying at each verification corner with OCV for mainly timing

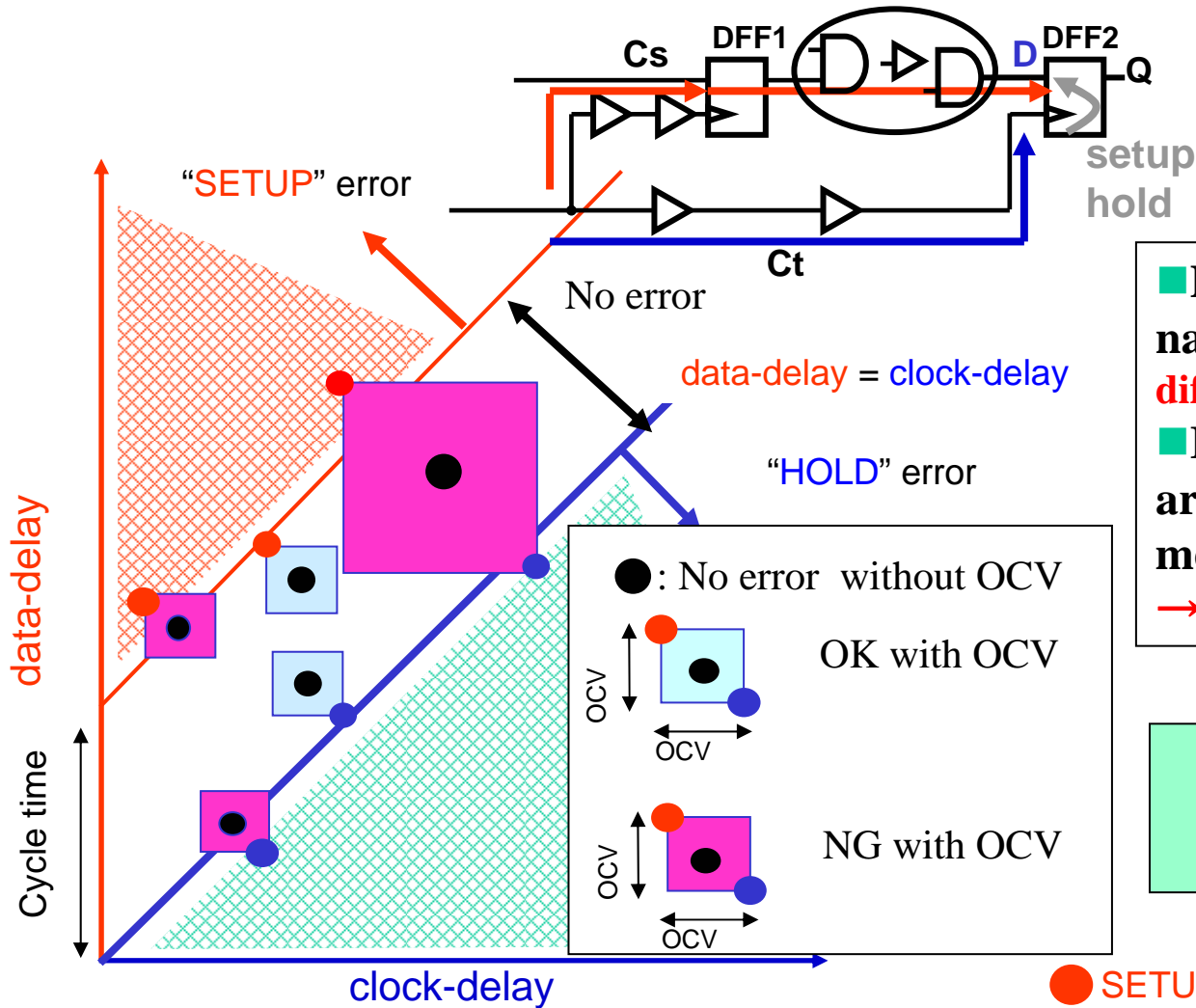
No methodology to define OCV value!!



Variation in process and design

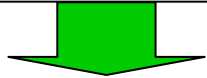


Difficulty in timing closure with OCV



■ Design window become more narrow with OCV → more difficult in timing closure

■ Future concern: No architecture in path with meeting setup and hold timing → Design impossible



What is true OCV value?

※assumption for simplifying : $FF(setup)=FF(hold)=0$

● SETUP check point
● HOLD check point

Summary

- STARCAD-21 is the state of the art design methodology for 90nm and below system LSI
- STARCD-21 is developed by collection of talent and experience in the Japanese semiconductor industry
- STARCAD-21 is applicable to real system LSI now
- STARCAD-21 is the de-facto standard design methodology
- STARCD-21 is expanding to support DFM