



Semiconductor Research Corporation®

PIONEERS IN
COLLABORATIVE
RESEARCH®

Design for Manufacturing: An SRC Perspective

Some Thoughts on DFM and Nanoelectronics

Ralph Cavin

Acknowledgements



- | | |
|-----------------------|--------------------|
| ◆ Luigi Capodieci | AMD |
| ◆ Dale Edwards | SRC/ AMD |
| ◆ Bill Joyner | SRC/ IBM |
| ◆ Andrew Kahng | UCSD |
| ◆ Andy Neureuther | U Berkeley |
| ◆ Walden Rhines | Mentor Graphics |
| ◆ Larry Pileggi | CMU |
| ◆ Vijay Pitchumani | Intel |
| ◆ Janusz Rajski | Mentor Graphics |
| ◆ Juan Rey | Mentor Graphics |
| ◆ Joseph Sawicki | Mentor Graphics |
| ◆ Christopher Spence | AMD |
| ◆ Andrzej Strojwas | CMU/ PDF Solutions |
| ◆ Chandu Viswesvariah | IBM |
| ◆ David Yeh | SRC/ TI |

DFM Philosophy



- ◆ Research in Nanodevices will have a value if and only if
 - ❖ We can find a way to cost-effectively make working circuits by connecting together TRILLIONS of such devices

- ◆ Nanoelectronics technologies require
 - ❖ a higher level of dialog between designers and process engineers on technology tradeoffs
 - ❖ An environment to facilitate these tradeoffs
 - ❖ New approaches to encoding information about design into material systems?

Outline



-
- DFM Principles How do DFM Principles apply to Nanoelectronics?
 - SRC research projects on DFM
 - Design for Self-Assembly?
 - A Review of Design for Manufacturing Guidelines

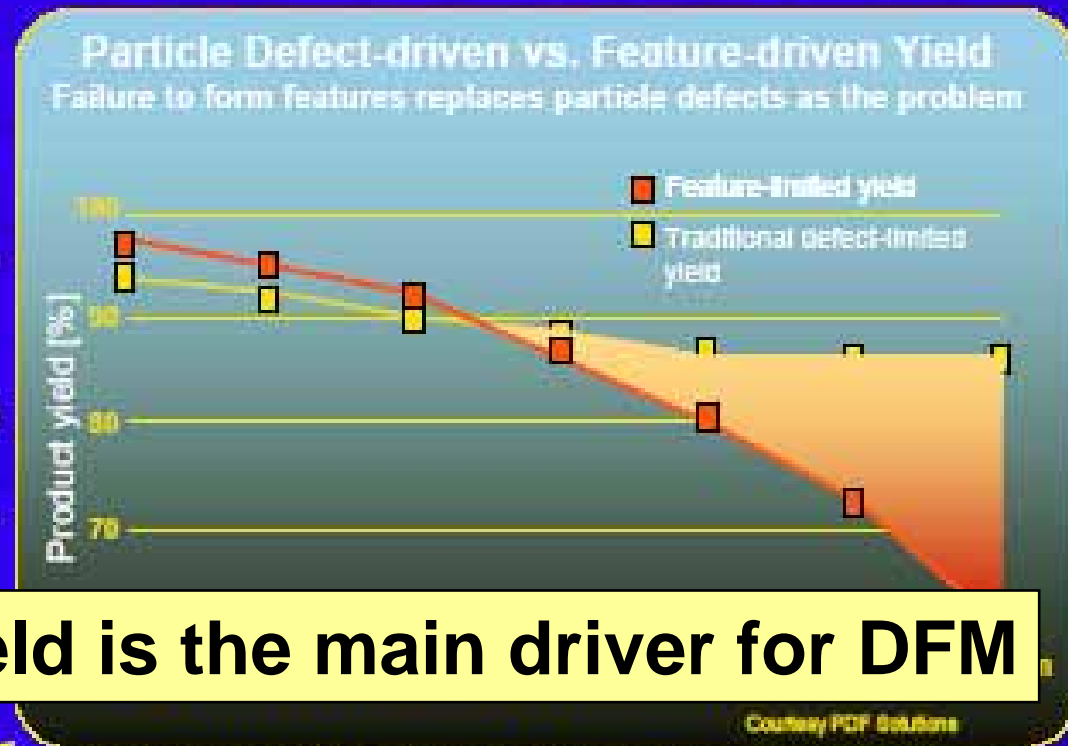
Design for Manufacturing Guidelines (Generic Conventional Wisdom)



- ◆ Reduce the number of parts and Minimize interconnections
- ◆ Standardize and use common parts and materials
- ◆ Avoid tight tolerances
- ◆ Design for ease of fabrication
- ◆ Design modular product

Yield

- Yield problems may be:
 - Catastrophic – Functional failure
 - E.g. bridging features, via failures
 - Parametric – Electrical parameter different than intended
 - E.g. Transistors faster (leakier) or slower
- Today yield is limited more by printability issues than by fab defects



Yield is the main driver for DFM

(Source: Dr. Bernd Koenemann, Mentor Graphics Corporation, ITC)

DFM is a Business Opportunity

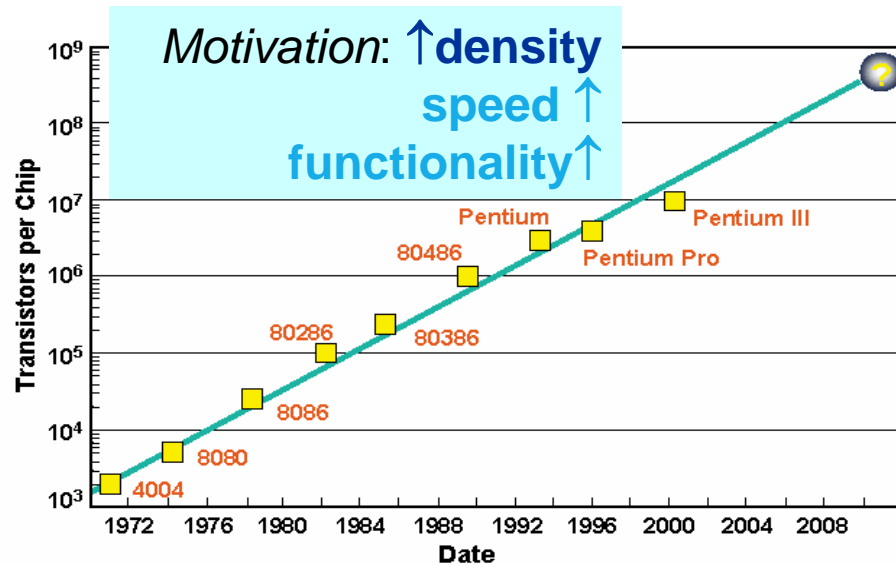
"Seamless" DFM Can Contribute 5% More Good Die



What's 5% more good die worth?

- ◆ \$50M over the life of a cell phone
- ◆ \$80M over the life of a game chip
- ◆ \$100M per year per fab at 90nm

Reduce the Number of Parts? NO



What is the ultimate number of binary transitions per second in a 1cm² chip area?

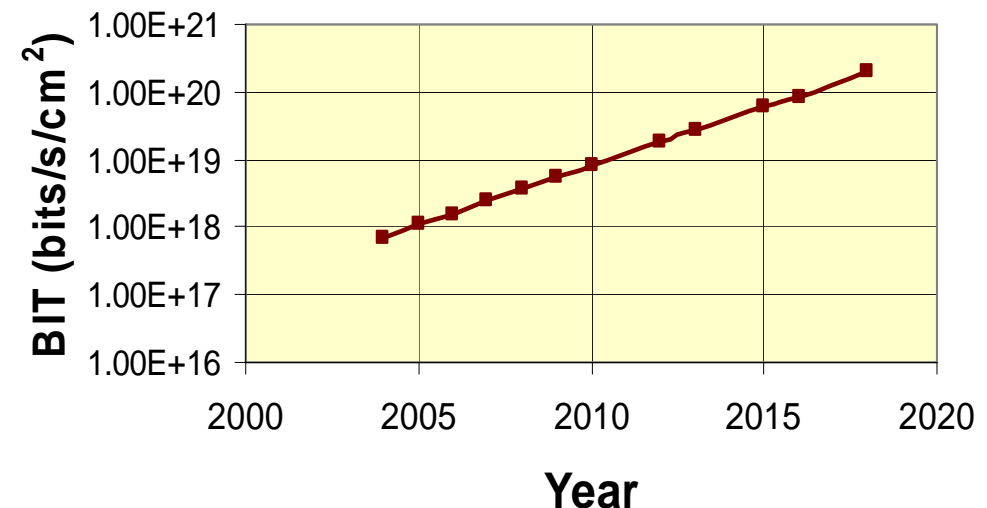
$$BIT = n_{bit} f$$

- a measure of computational capability on device level

n_{bit} – the number of binary states
 f – switching frequency

Source: Stan Williams, Hewlett Packard

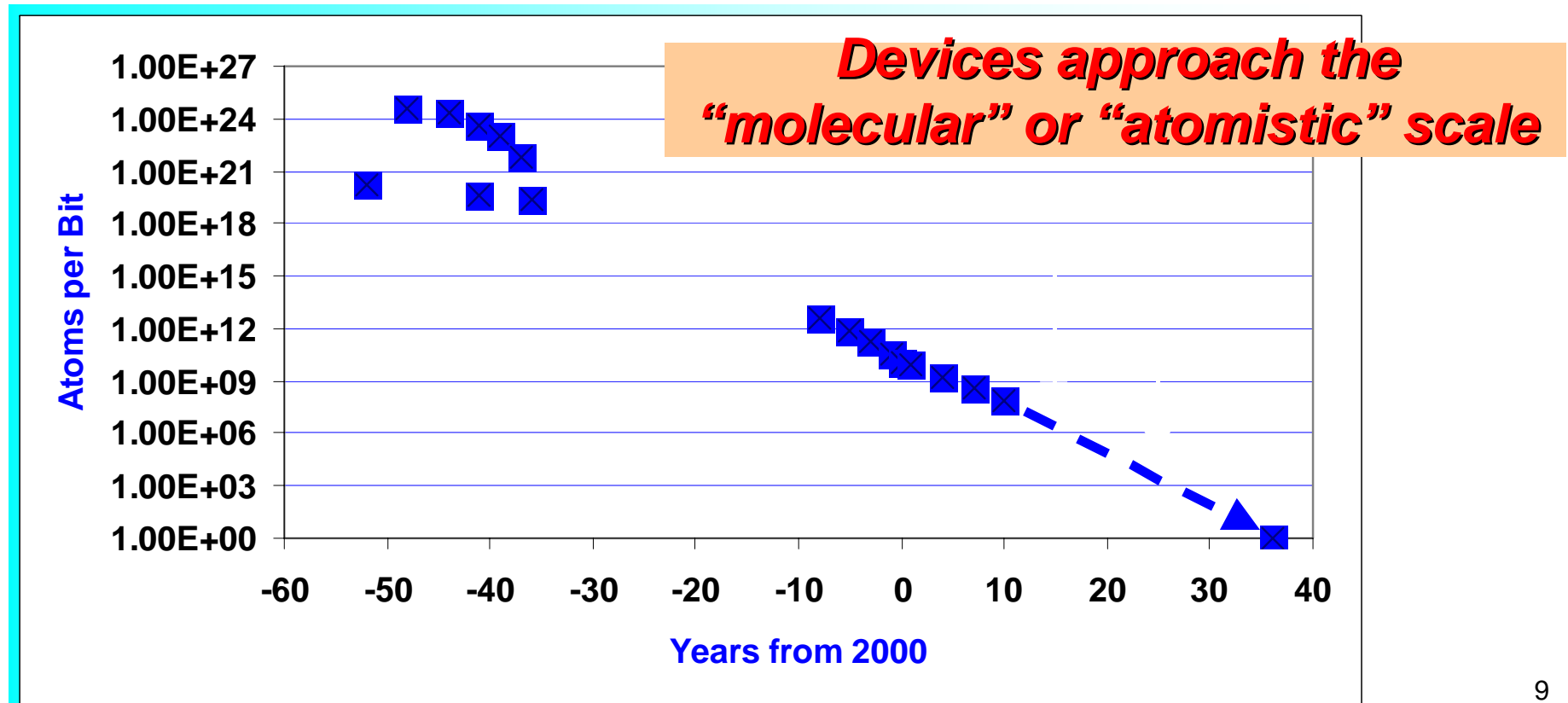
Why scaling? – To increase the *Binary Information Throughput* (BIT)



Avoid Tight Tolerances



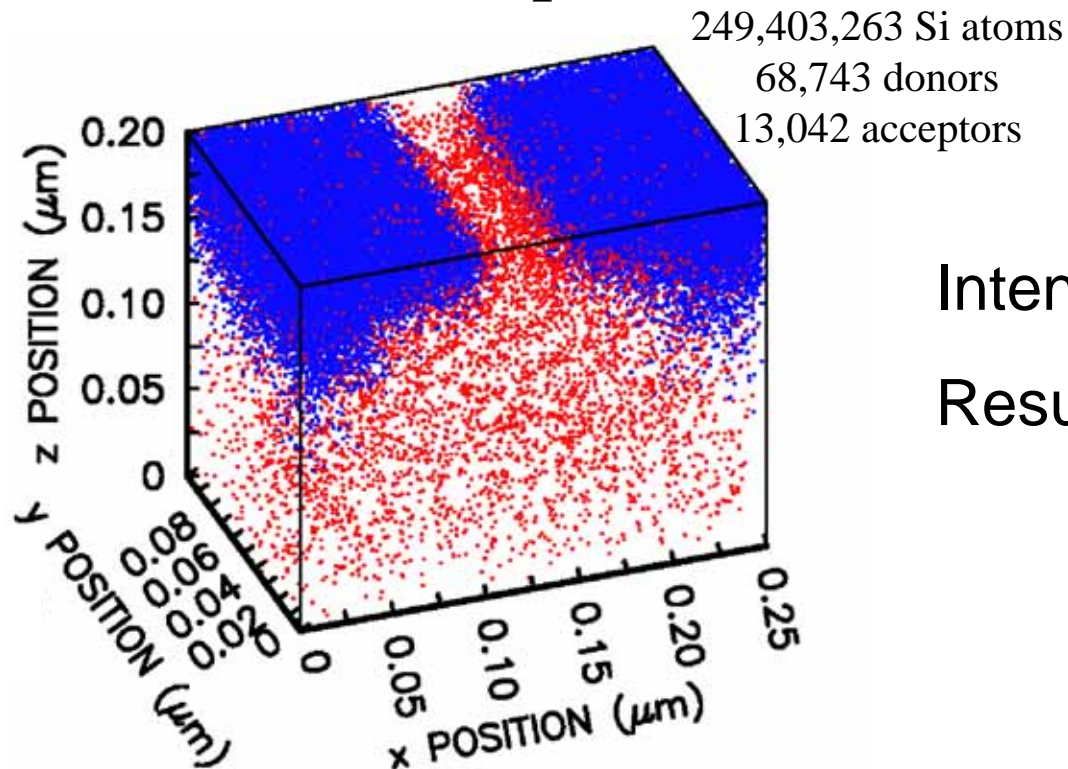
One reason why the variability increase in IC performance is UNAVOIDABLE, is the Statistical \sqrt{N} Effect: The physical parameters of a system of N atoms are inaccurate within a probable relative error of the order of $\frac{1}{\sqrt{N}}$



Variability is increasing



Discrete dopants



Intended: N

Resulting: $N \pm \sqrt{N}$

D. J. Frank et al, Symp. VLSI Tech., 1999

© Chandu Visweswariah, 2004

Statistical Analysis and Design: From Picoseconds to Probabilities

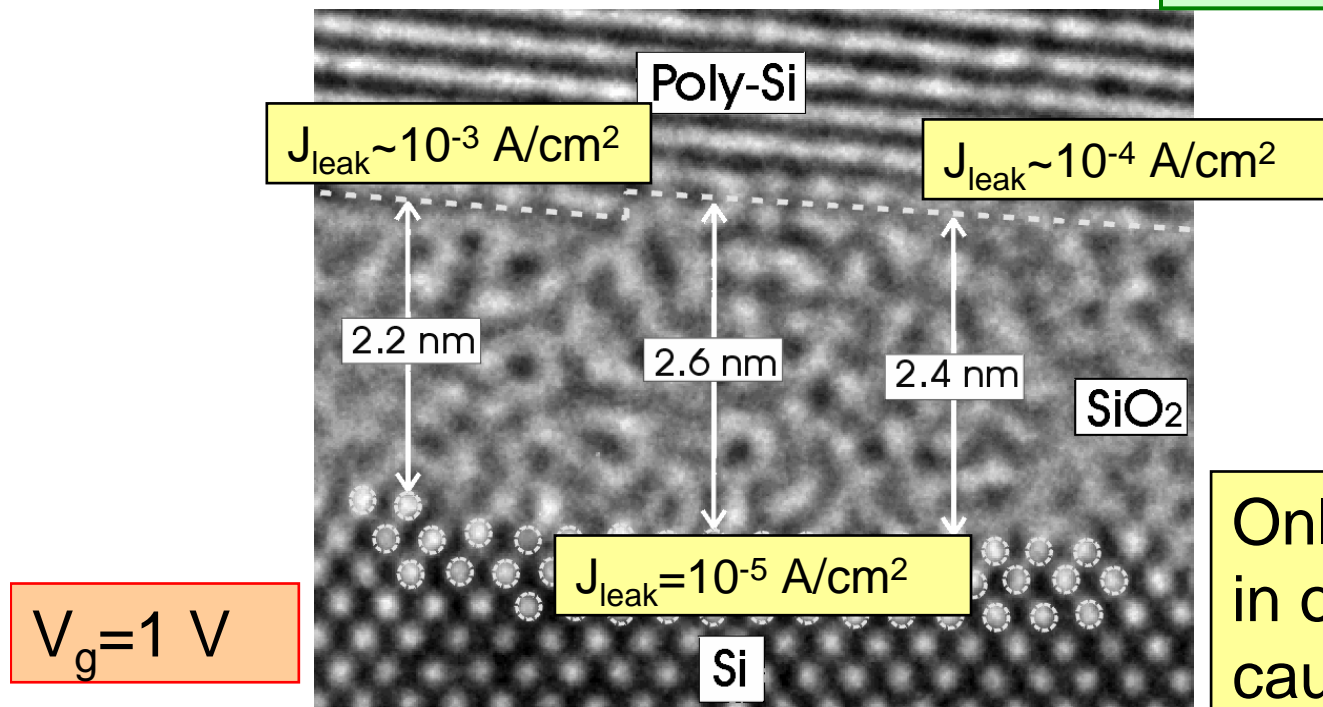
3 of 86

Variability is increasing



Oxide variations

$$J_{leak}(t_{ox}) \sim \exp\left(\frac{2\sqrt{2m\phi_B}}{\hbar} \cdot t_{ox}\right)$$

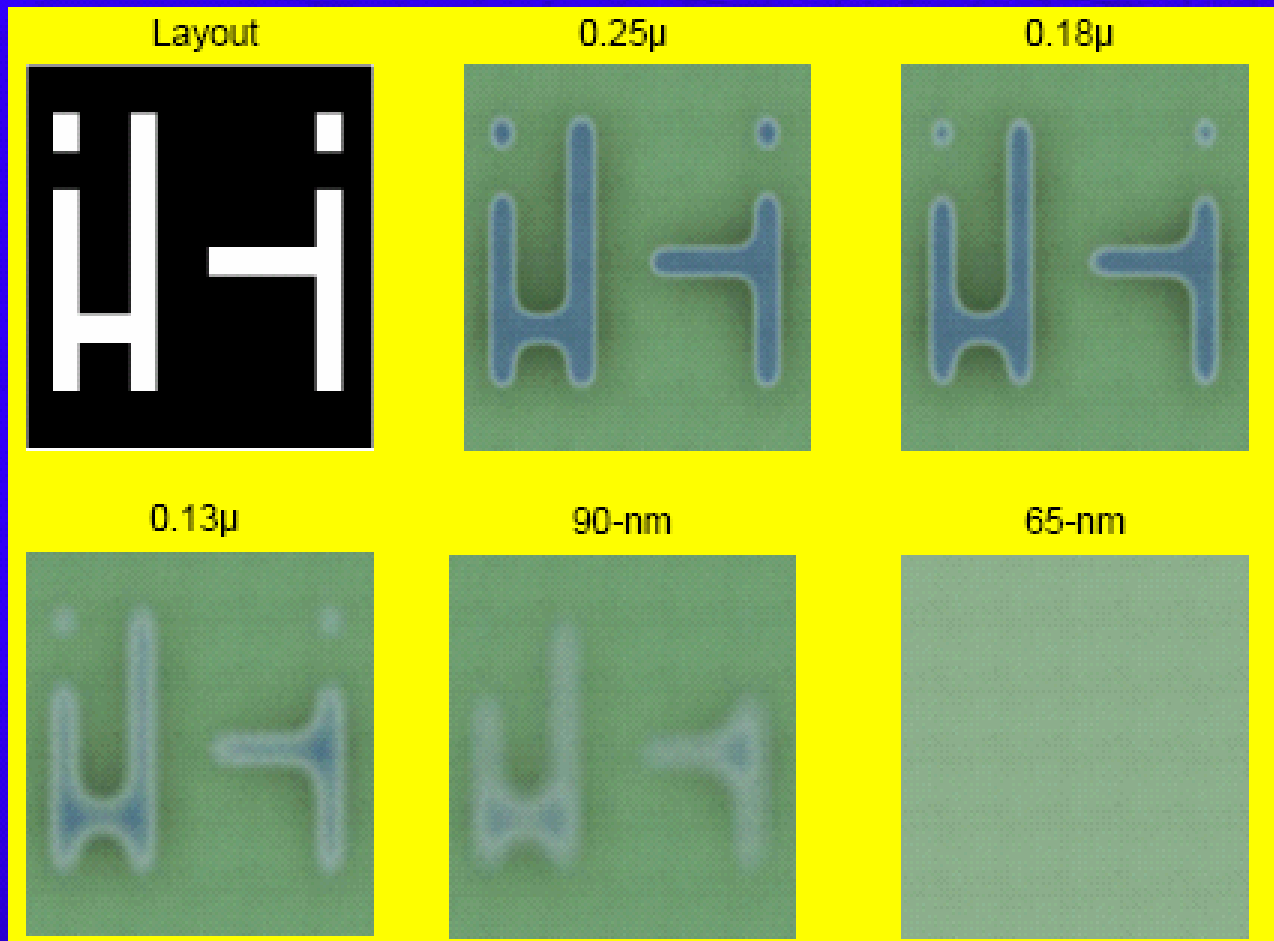


Only 0.2 nm of variation in oxide thickness causes one order of magnitude variation in leakage

OEC can help but ultimately
can't forestall the inevitable



Drawn vs. printed mismatch grows



intel

(Source: Andrew Kahng's ICCAD 2003 tutorial)

Figures courtesy Synopsys Inc.

A Review of Design for Manufacturing Guidelines as Applied to IC's



- ◆ Reduce the number of parts/Minimize interconnections ?
 - ❖ NO
- ◆ Standardize and use common parts and materials?
 - ❖ Already done in CMOS, MUST BE implemented in the post-CMOS nanoelectronics research
- ◆ Design for ease of fabrication?
 - ❖ DESIGN FOR SELF-ASSEMBLY?
 - ❖ Self-Correcting Circuitry
- ◆ Avoid tight tolerances?
 - ❖ YES!!! STATISTICAL DESIGN?
- ◆ Design modular product?
 - ❖ YES: Extreme Layout Regularity

Design for Manufacturing:

Examples of SRC research projects



- ◆ Avoid tight tolerances
 - ❖ *Designing with Unreliable Components at the Scaling Limit*
 - ❖ *Diagnostic Reasoning for Performance Failures Considering Realistic Noise, Process Variations, and Defects*
 - ✓ ❖ *Optimization of Lithographic Induced Variability for Improved Circuit Performance*
- ◆ Design for ease fabrication
 - ✓ ❖ *Modeling Nanoscale Phenomena for Maskless Lithography*
 - ❖ *Modeling Within-Die Variation and Spatial Correlation Effects for Process/Design Optimization*
 - ✓ ❖ *Integrated Framework for Reliability- and Process-Variation Aware Design Methodology for VLSI Circuits*
- ◆ Design modular product
 - ✓ ❖ *Circuit Primitives for Regular Logic Bricks*
 - ❖ *A Formal Methodology for Probabilistic Design of Robust Nanometer Scale Digital Circuits*

Optimization of Lithographic Induced Variability for Improved Circuit Performance



David Blaauw

Michigan

- ◆ Process-induced variability has caused increasing uncertainty in chip-level performance, even with advanced and costly RET
- ◆ Research is developing new approaches to improve overall circuit performance by tuning RET and equipment parameters and exploring new circuit design styles and layout practices less sensitive to process variations
- ◆ Method assures connection to *performance*

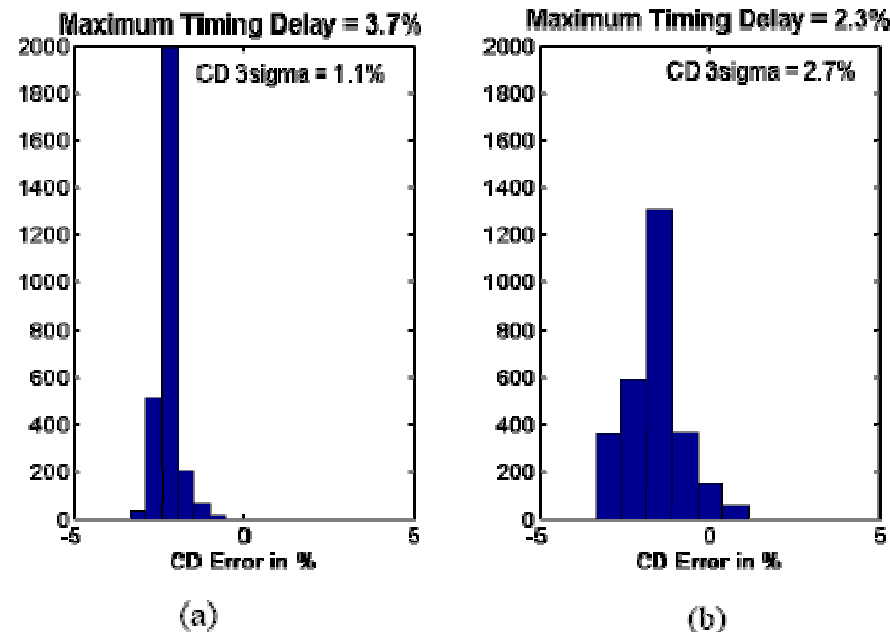


Figure 2. Circuit level impact of CD control. Contrary to intuition, the setting leading to less well controlled CD distribution shown in (b) resulted in better overall circuit performance.

Integrated Framework of Reliability and Process-Variation Aware Design of VLSI Circuits

Mohammad Alam and Kaushik Roy

Purdue



- ◆ DFM based on both spatial and time variant process parameters
- ◆ Develops models for time and stress dependent parameter drifts
- ◆ Develops a sizing tool using Lagrangian relaxation algorithm for global optimization of transistor widths
- ◆ Work will consider time dependent parameter shifts from all degradation sources
- ◆ Preliminary benchmarks show savings of 20% area while maintaining the same yield and performance
- ◆ Primary output – design toolkit and Spice models

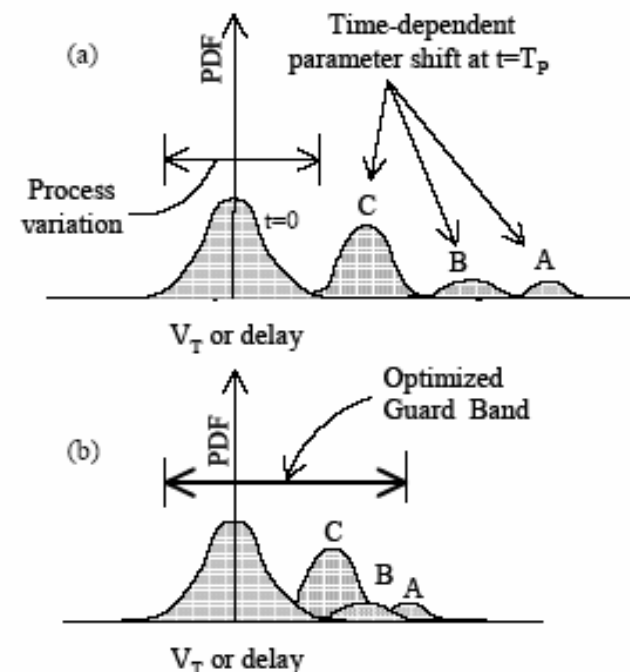


Fig. 2: (a) Depending on the switching history, transistors have different degrees of parameter drifts. (b) The circuit can be redesigned for optimal performance if the time-dependent shifts and process-variations are well-characterized.

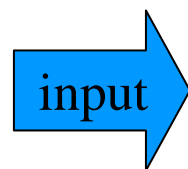
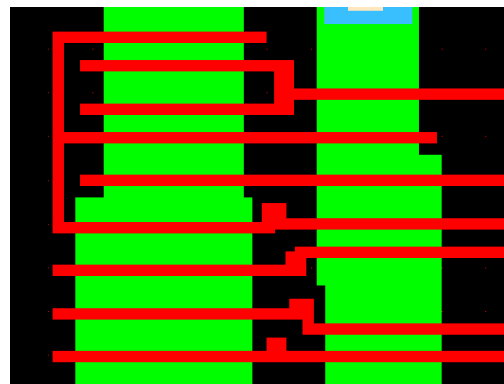
Modeling Nanoscale Phenomena for Lithography

Neureuther Berkeley

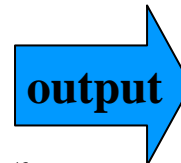


Experiments/Simulation to identify how layouts impact yield

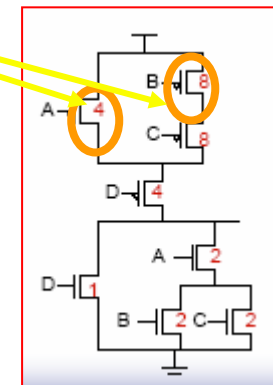
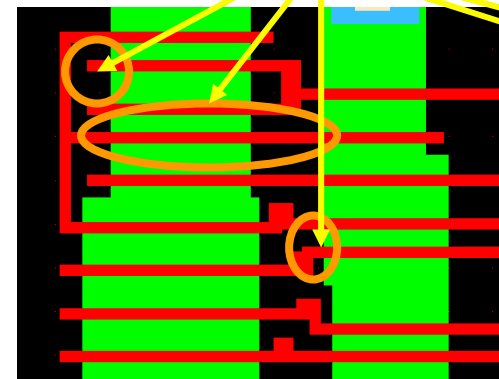
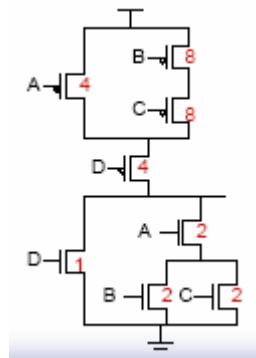
Focus	Dose	Power
-0.2	20	17
-0.1	20	15
0	20	14
0.1	20	14
0.2	20	15
-0.2	21	20
-0.1	21	19
0	21	16
0.1	21	22
0.2	21	24



Yield Simulator



Source of leakage problem



Circuit analysis allows us to ignore transistor 6 and 7 even though they have a lot of leakage variation

Circuit Primitives for Regular Logic Bricks

Larry Pileggi

CMU



- ◆ Research proposes to derive the set of fixed size transistor/logic primitives to build the most efficient regular logic bricks for implementation of digital circuits in nanoscale technologies
- ◆ By introducing restrictive design rules, RET-correct designs can be created by construction
- ◆ A design flow that guarantees geometrical regularity by way of a small collection of regular logic structures will be used
- ◆ Minimal impact to area and performance

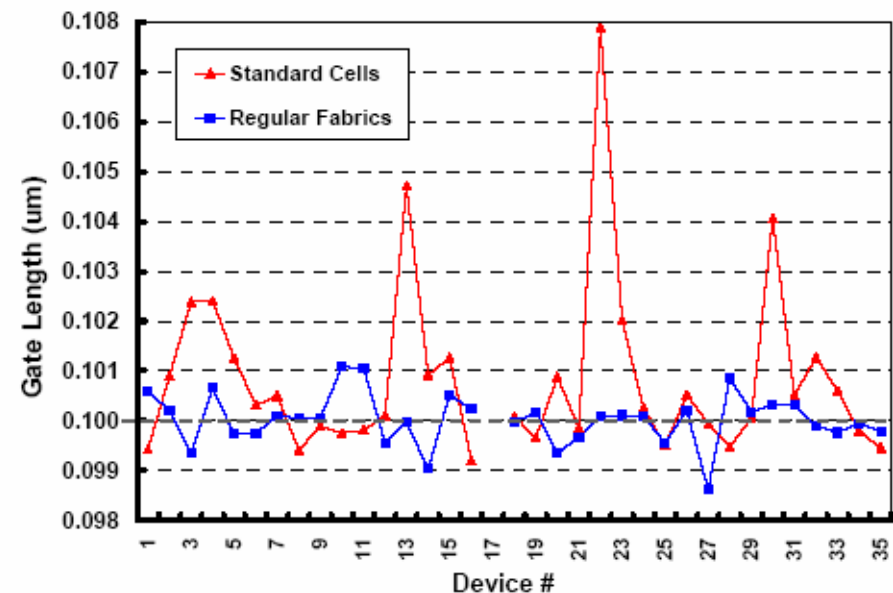


Figure 1 : Polysilicon gate length variations comparison.



Semiconductor Research Corporation®

PIONEERS IN
COLLABORATIVE
RESEARCH®

Design for ease fabrication

DESIGN FOR SELF-ASSEMBLY?

Energetics of Patterning and Manufacturing Defects



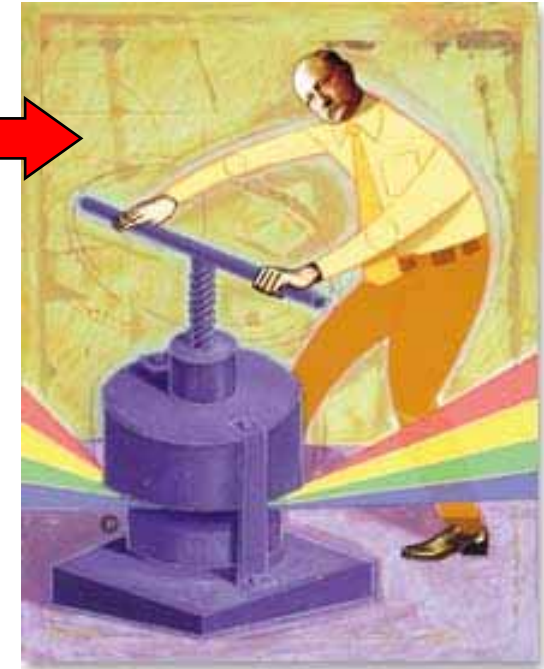
Feature size is inversely related to the energy of information carrier:

$$\lambda = \Delta L(\text{tolerance}); e.g. \Delta L = 0.5L$$

$$E = \frac{hc}{\lambda} = \frac{hc}{\Delta L} = \frac{2hc}{L}$$

$$L = 5 \text{ nm}$$
$$E > 500 \text{ eV}$$

We are using brute force



Energy density absorbed by substrate (throughput 1 cm²/s):

$$P = E_{ph} \cdot n_{ph} = \frac{2hc}{L} \cdot \frac{4}{(L)^2} = \frac{8hc}{L^2} = 51 \frac{\text{W}}{\text{cm}^2}$$

It is very hot!

Bond Energy in Solids: 3-8 eV << 500 eV

Since the energy to 'print' far nanometer regime features far exceeds the bond energy of solids, defects from printing are inevitable

Manufacturing is Information Transfer

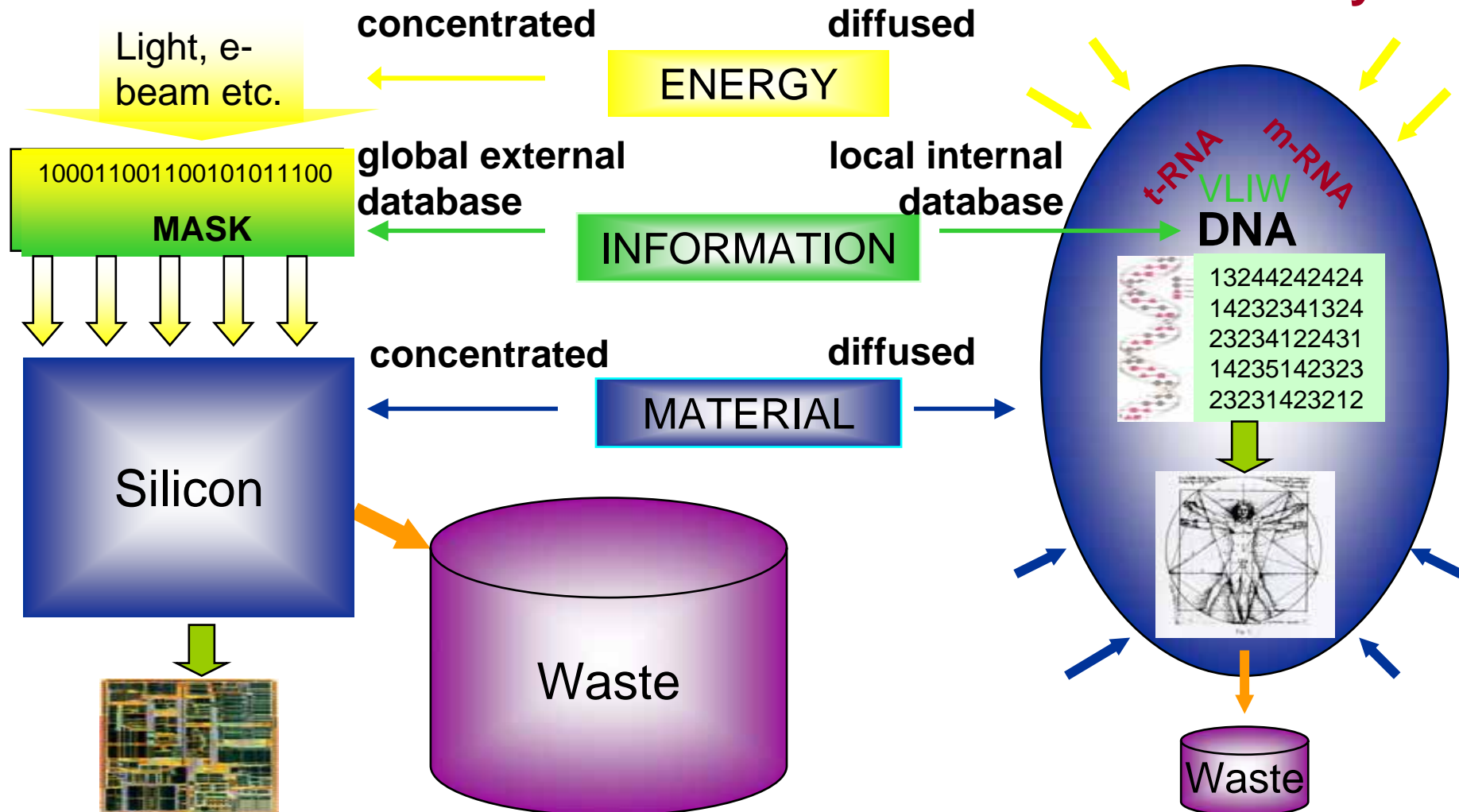
- Foundational knowledge base is needed



Complex Matter=Energy+Information+Material

Subtractive

Assembly



Energetics of Assembly: Biological Inspiration



The 9-month development of a newborn:

*Conventional Subtractive
Manufacturing:
Energy per atom*

$$\epsilon_{total} = 2 \times 10^{-15} \frac{J}{at}$$

Assembly with less
energy would ease
manufacturing
constraints

Input:

- Weight of newborn $m=3$ kg
- Composition: 70% H_2O + 30% $C_3H_6O_2N$ (amino acids)
- Additional calories for pregnant woman: **300 cal/day**
- Time: 9 month

Calculation:

- Total additional energy of pregnancy: $E=300cal/day * 4.18J/cal * 9mon * 30day/mon = 338580 J$

- Number of assembled molecules:

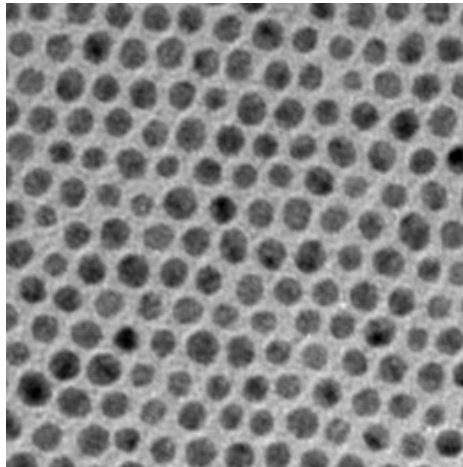
$$N = \frac{N_A}{M} m = 4.62 \times 10^{25}$$

- Energy per assembled molecule: $\epsilon = \frac{E}{N} = 7.34 \times 10^{-21} \frac{J}{molecule}$

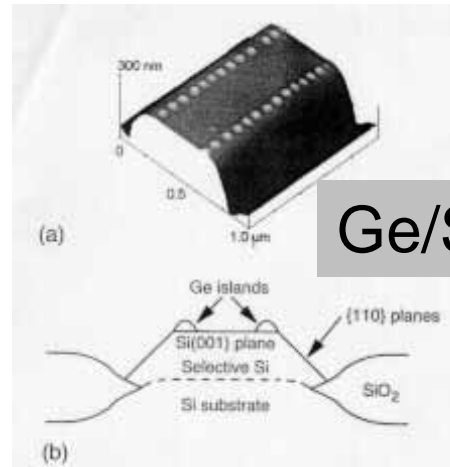
- Assembly rate: **$N/t = 2 \times 10^{18}$ molecule/s**

Assume a transistor occupies a volume of $\sim 1 \times 10^6$ nm³, corresponding to $\sim 50M$ silicon atoms. At biological growth rates, a 1Gb chip could be built in about 5 s.

Regular arrays of simple elements can be produced by self-assembly driven by equilibrium thermodynamics

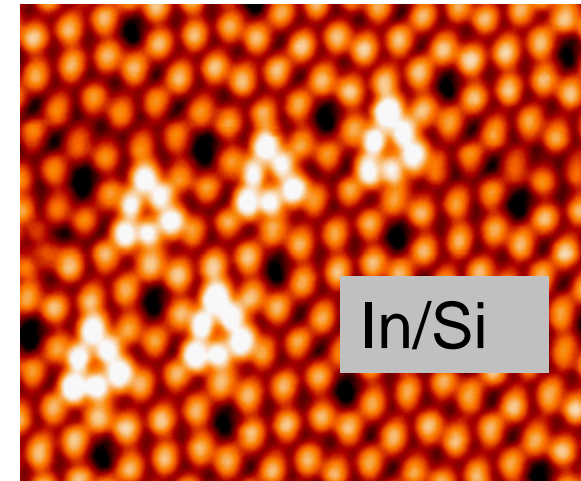


Self-Assembled 2-D array of Au clusters, (D. Janes/Purdue)



Ge/Si

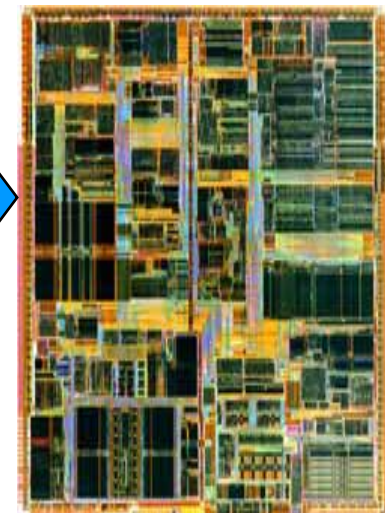
T.I. Kamins and R.S. Williams, Appl. Phys. Lett. 71 (1997)



In/Si

Li et al, Phys. Rev. Lett. 88 (2002)

However, we need very complex structure with very high information content – *We need to tell atoms where to go*



Our understanding of self-organization is embryonic

Can we encourage matter to assemble into a structure we want?



The key task is to find the information sources and channels to convey the assembly instructions. For example, can we learn secrets of living matter to build things?

Sources of Information for self-organization of complex structures:

Time-dependent environment parameters (non-equilibrium processes)
Embedded Code (e.g. DNA)
Fundamental Constants: DNA of Universe?

“We have no theory, that gives us a metric for the information embodied in a physical structure...This missing metric (may) be the most fundamental gap in the theoretical underpinnings of information science”.

Frederick Brooks (IBM 360 Architect, currently UNC Chapel Hill), 2003

How would Self-Assembly Change the DFM Equation?



- ◆ If we can find a way to encode assembly information into a process from the bottom-up, the belief is that we can more precisely control the location of each material particle.
- ◆ Would designers encode designs in DNA-like descriptors?
- ◆ The process engineers task would be to create a precisely controlled process environment into which the design information is inserted
- ◆ Speculative but would design simultaneously embrace process and DNA design?

Conclusions



- ◆ DFM is driven by production yield difficulties in developing new generation of devices and circuits.
- ◆ Division between fabless and fab means that a lot of communication between design and process development that used to take place is not taking place.
- ◆ A zillion start-ups are offering solutions but it is not clear yet what the real problems are and it is likely that when the key problems are identified that fundamentally new approaches will be required.

Conclusions

- ◆ When considering sources of variations there are several problems in identifying the fundamental physical causes. Little data is available, and there is poor communication of information.
- ◆ While we have good underlying physical models of individual effects we have yet to build the knowledge base to do predictive simulation and EDA.
- ◆ Communication of possible solutions is an issue as design rules may not be an adequate basis for expressing solutions to the problem and fewer designers are talking to technologists.
 - ❖ With more companies going fab-less there is even weaker communication.
- ◆ The process technology is going to get even more complex.

Possible Agenda for Collaboration



- ◆ Can we define real problems by sharing pre-competitive data?
- ◆ Develop a framework for a synergism between circuit design and process control?
- ◆ Instead of doing it empirically develop first-principle methods to comprehend DFM variation issues?
- ◆ Form an International Consultative Working Group to coordinate fundamental research in self-organization for nanoelectronic manufacturing with an emphasis on design?

Acknowledgements



- ◆ Luigi Capodieci AMD
- ◆ Dale Edwards SRC/ AMD
- ◆ Bill Joyner SRC/ IBM
- ◆ Andrew Kahng UCSD
- ◆ Andy Neureuther U Berkeley
- ◆ Walden Rhines Mentor Graphics
- ◆ Larry Pileggi CMU
- ◆ Vijay Pitchumani Intel
- ◆ Janusz Rajski Mentor Graphics
- ◆ Juan Rey Mentor Graphics
- ◆ Joseph Sawicki Mentor Graphics
- ◆ Christopher Spence AMD
- ◆ Andrzej Strojwas CMU/ PDF Solutions
- ◆ Chandu Viswesvariah IBM
- ◆ David Yeh SRC/ TI