

# Panel Session

## Devices and Technologies for hp32 and Beyond

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### Moderator:

**Toshiro Hiramoto**  
**James A. Hutchby**

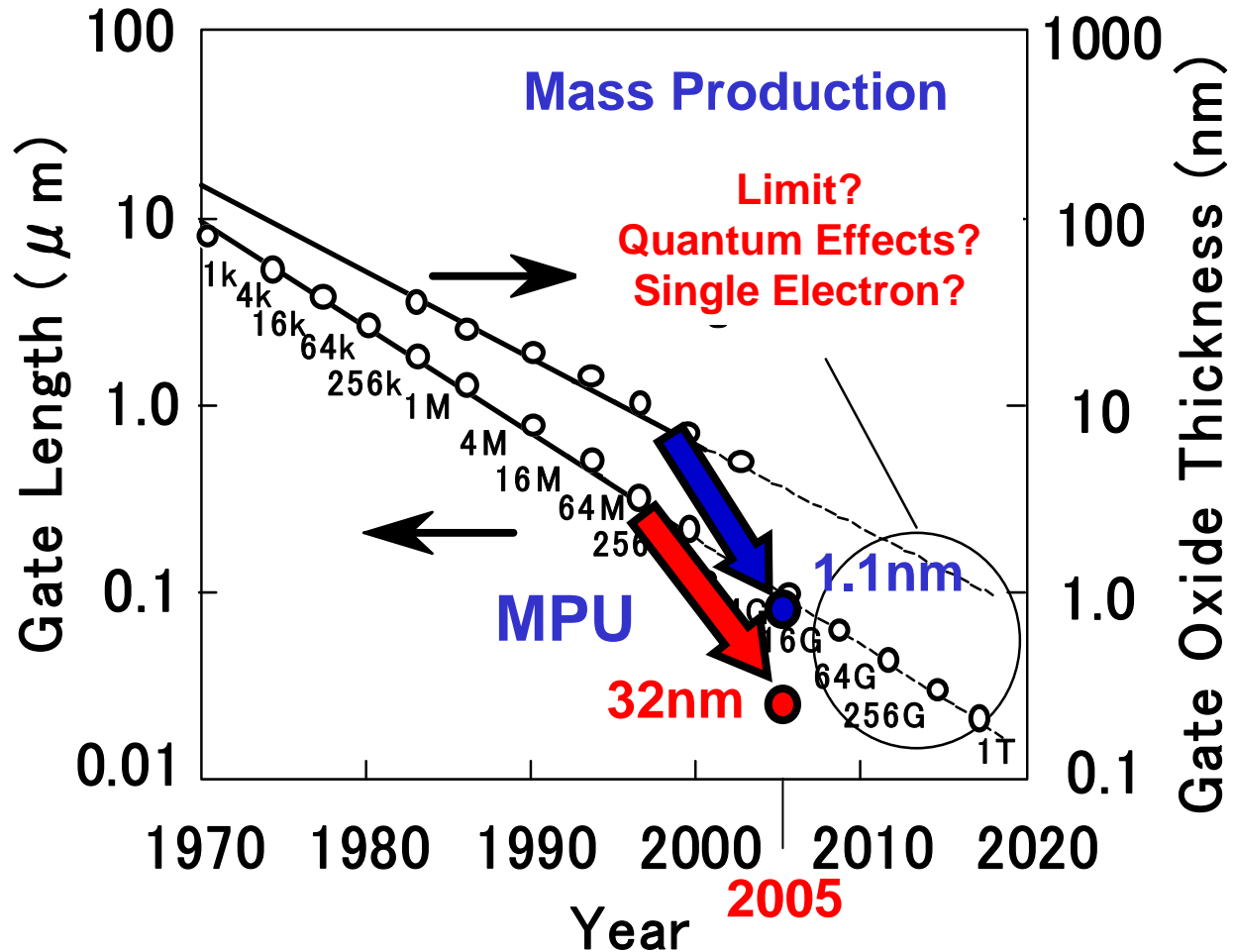
**University of Tokyo, Japan**  
**SRC, USA**

### Panel:

**MeiKei leong**  
**Simon Deleonibus**  
**Judy L. Hoyt**  
**Makoto Yoshimi**  
**Kazunari Ishimaru**

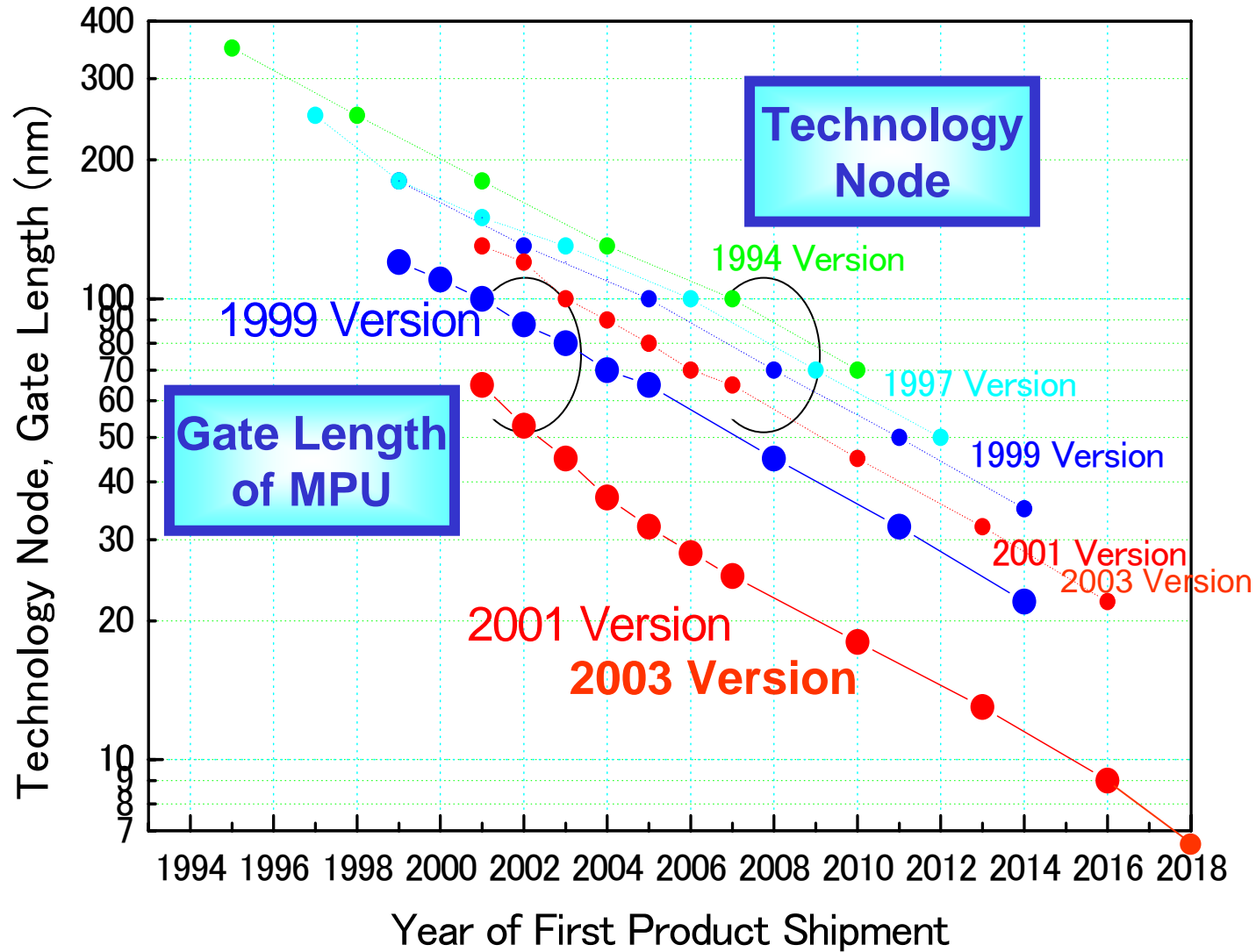
**IBM, USA**  
**LETI, France**  
**MIT, USA**  
**SOITEC Asia, Japan**  
**Toshiba, Japan**

# Trend of MOSFET Scaling



The VLSI MOS devices are already in the nano-scale regime!

# Roadmap: Gate Length of MPU



# Non-Classical CMOS

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**Non-Classical CMOS provides a path to scaling CMOS to the end of Roadmap using new transistor structural designs and new materials.**

## **Scaling challenges:**

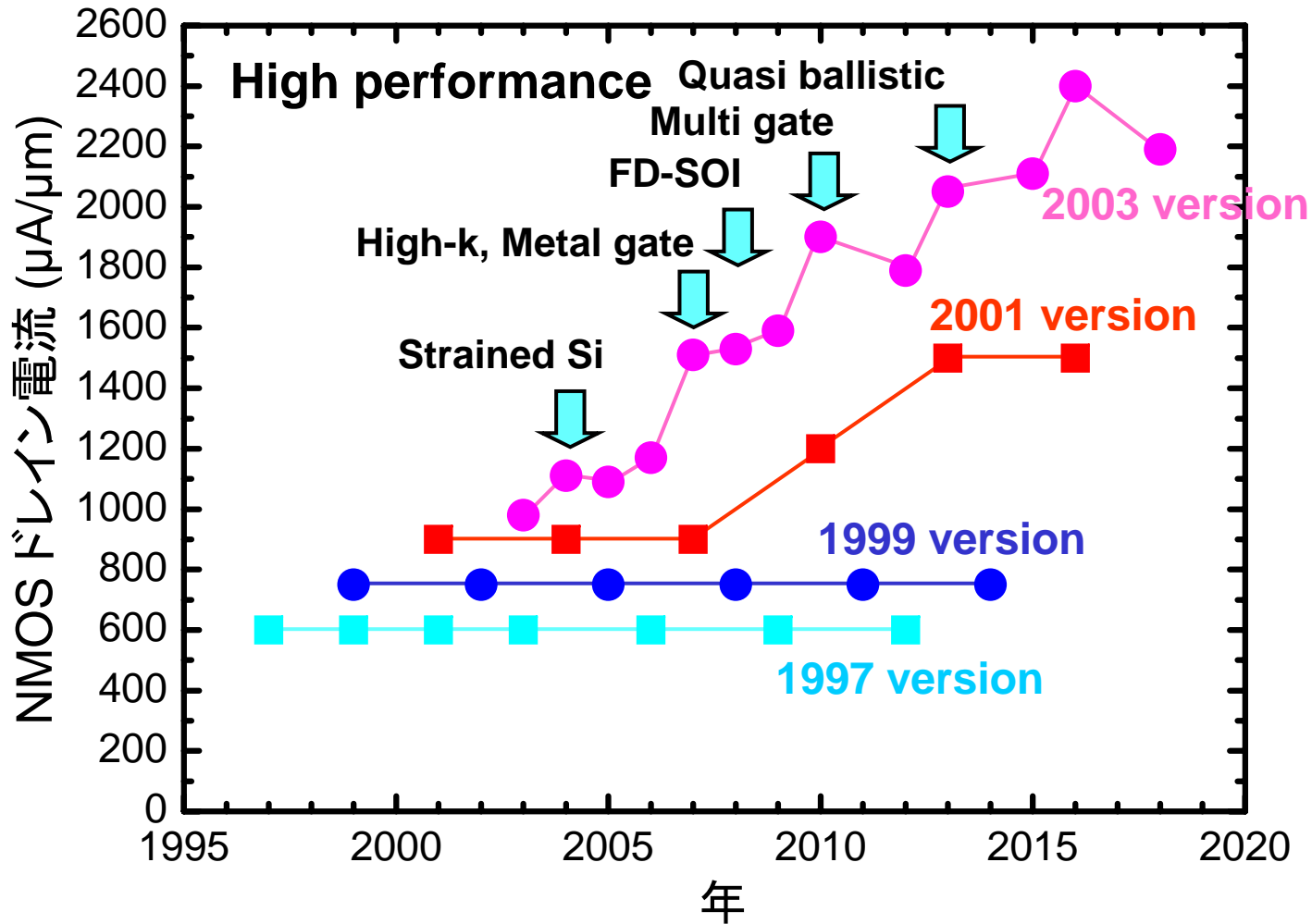
- **Increasing saturation current while reducing the power supply**
- **Controlling leakage currents and short-channel effects**
- **Control of device parameters across the chip and from chip to chip**

## **Two major approaches**

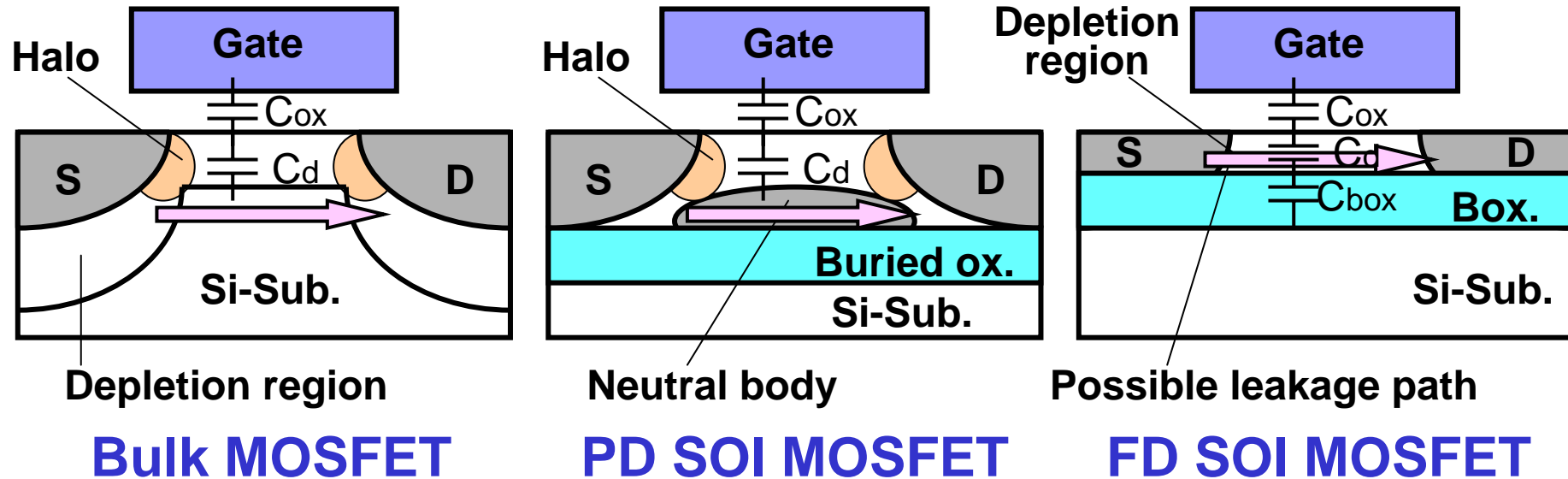
- **New materials: improve carrier transport properties**
- **New transistor structures: improve the electrostatics of MOSFETs**

**2003 ITRS**

# Trend of Targeted Ion in ITRS



# Bulk and SOI MOSFETs



## - Suppression of Short Channel Effect

Stronger gate control

Gate should be as close to the leakage path as possible.

## - Small S factor $\rightarrow S \sim 60 (C_{ox} + C_d) / C_{ox}$

Ultra-thin-body FD SOI MOSFETs promising.

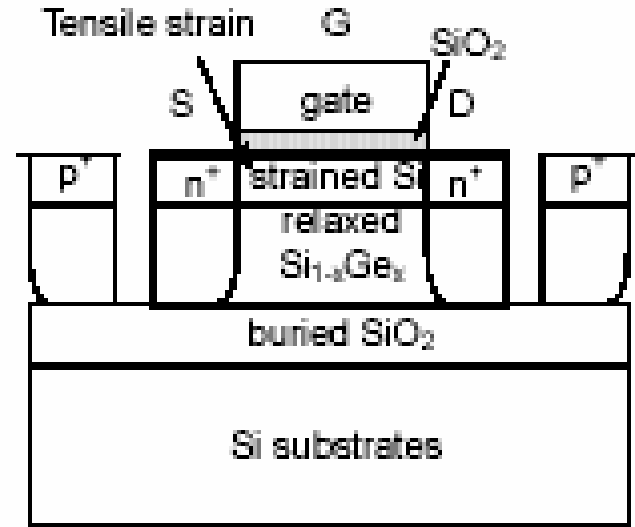
(Small SCE and Small S factor at the same time)

# Strained Si

## Biaxial Strain

- Global strain in Si/SiGe
- Mobility enhanced both in electron and hole

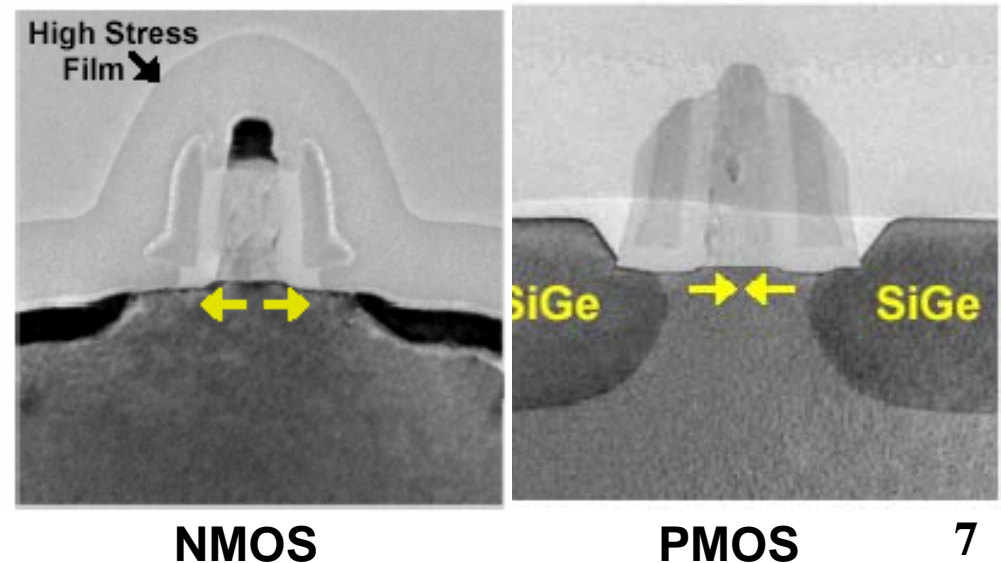
S. Takagi, 2003 IEDM.



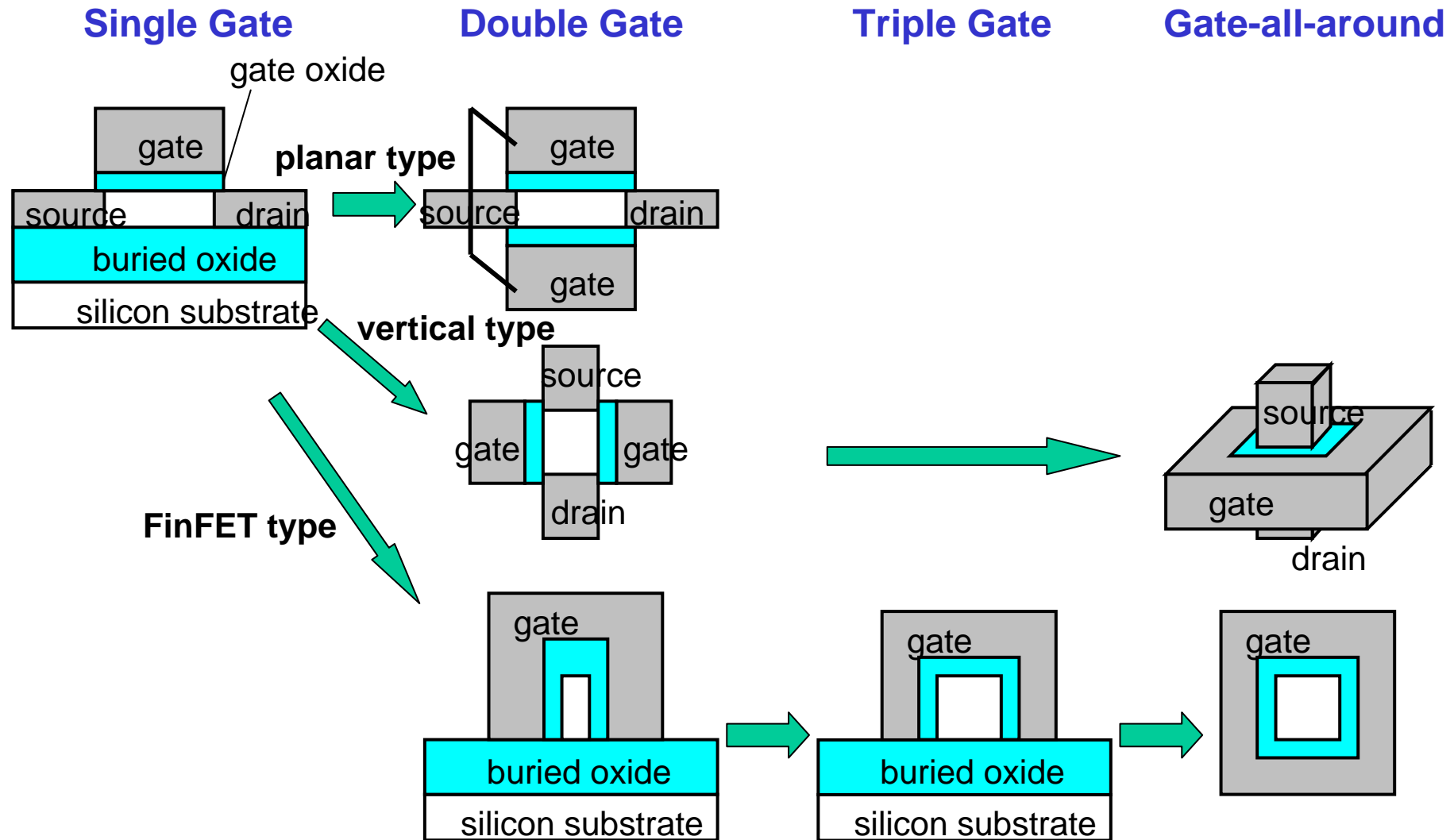
## Uniaxial Strain

- Local strain during process
- SiN liner
- Embedded SiGe in S/D

T. Ghani, 2003 IEDM.



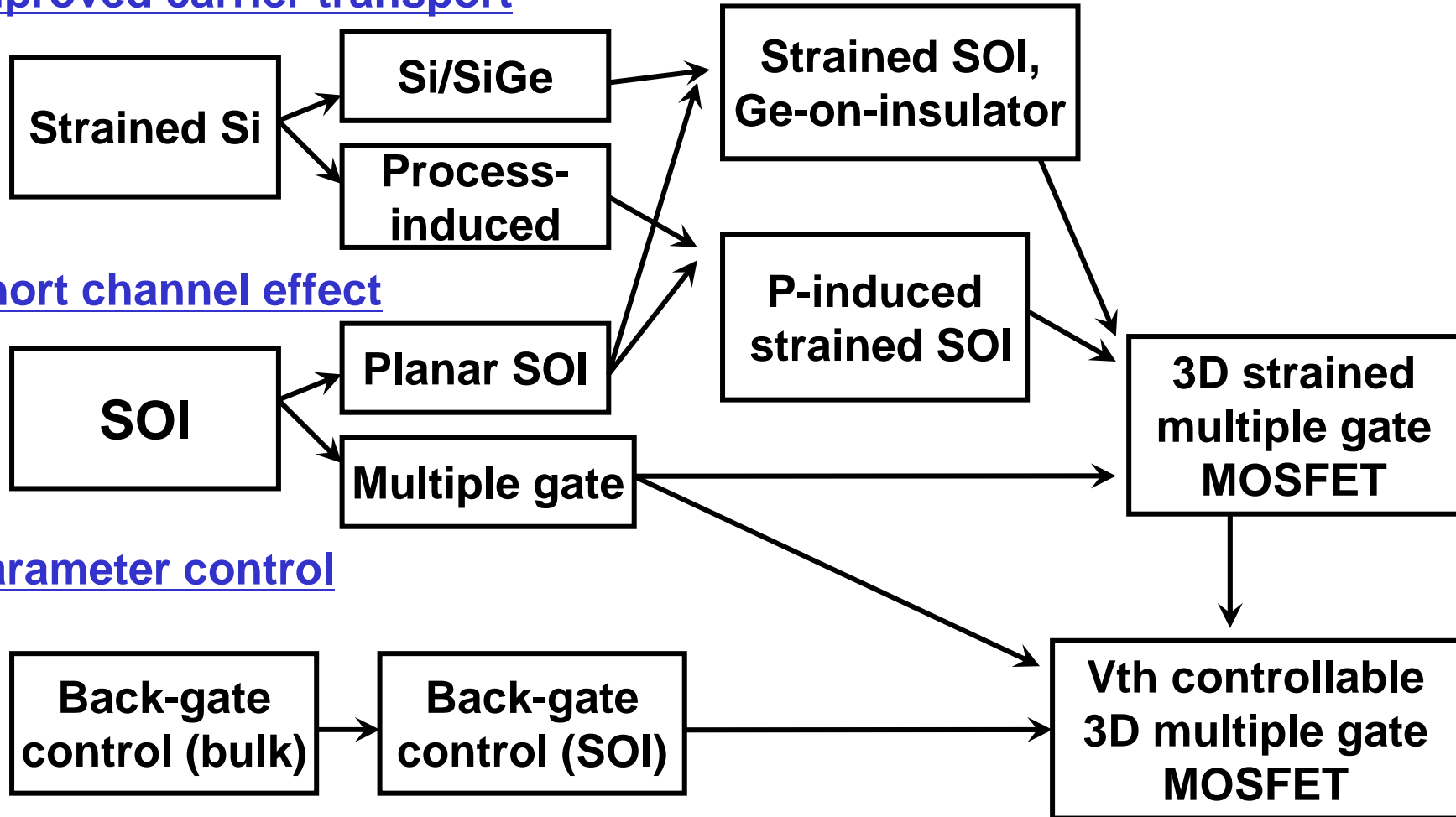
# Evolution of Multi-Gate MOSFETs





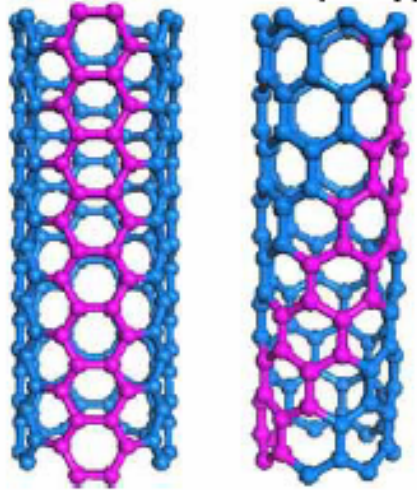
# Nano CMOS Evolution

## Improved carrier transport



# Nanowires and Nanotubes

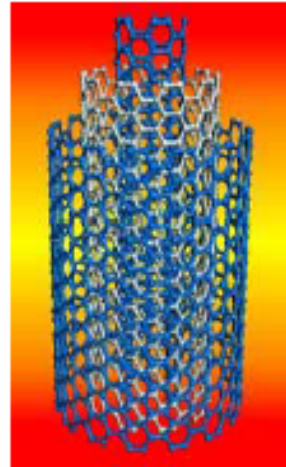
SWNT  
armchair zigzag



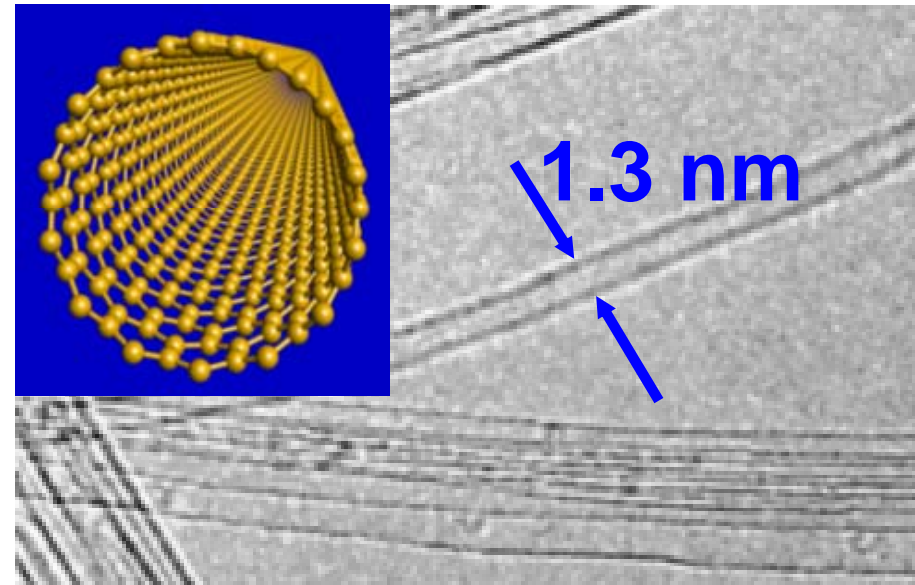
metal

Semicond.  
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MWNT



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**Applications:**

**FETs**

**Interconnects**

# Questions

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- Q1 Bulk or planar SOI, and when?**
- Q2 FinFET or tri-gate, and when?**
- Q3 Global strain, local strain, or other techniques, and when?**
- Q4 For High-performance or low-power applications?**
- Q5 Si nanowire, carbon nanotube FET, or other new devices, and when?**

# Summary

Tech. node	65nm	45nm	32nm	22nm	15nm	11nm
Half pitch	hp90	hp65	hp45	hp32	hp22	hp15
leong	Bulk					
Deleonibus	Bulk					
Hoyt	Bulk					
Yoshimi	Bulk					
Ishimaru	Bulk					
Audience	Bulk					
Year	2005	2007	2010	2013	2016	2019



