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IFST 2005 Panel Discussion Devices and Technologies for hp32 and Beyond

Meikei leong
June 21, 2005

" Devices and Technologies for hp 32 and beyond "

Semiconductor companies are now ready for the introduction of the 65 nm technology , and the focus of the device research and development is moving to the next generations . The basic device concepts , including the choice of structures and materials , are being established for the 45 nm technology . However , there are issues of controversy for the 32 nm technology and beyond in regards to which device structure is the best choice , when the new device structures such as a FinFET should be introduced in production , and what kind of devices should be selected for each application . The technology choice largely depends on applications and the technology generation . Moreover , new devices such as a silicon nanowire FET and a carbon nanotube FET , are emerging . At this panel session , it is our goal to focus our attention on the devices and technologies for hp32 and beyond discussing the pros and cons on various device structures and expanding the outlook of the future device technology .

- Bulk or planar SOI ? FinFET or tri - gate , and when ?
- Global strain , local strain , or other mobility enhancement techniques ?
- High - performance or low - power applications Si nanowire FET , carbon nanotube FET , or other new devices
- Moderator :
- Toshiro Hiramoto University of Tokyo , Japan James A . Hutchby SRC , USA
- Panel :
- Simon Deleonibus LETI , France
- Judy L . Hoyt MIT , USA
- MeiKei leong IBM , USA
- Kazunari Ishimaru Toshiba , Japan
- Makoto Yoshimi SOITEC Asia , Japan

Roadmap

Technology	65nm node 2006-07?	45nm node 2008-10?	32nm node 2010-13?	22nm node 2012-16?	15nm node 2014-19?
High performance (HP)	B-PD	B-PD	FD/Fin	FD/Fin	FD/Fin
Low operating power (LOP)	B-PD	B-PD	FD/Fin	FD/Fin	FD/Fin
Low standby power (LSTP)	B-PD	B-PD	B-PD	FD Fin	FD/Fin
Other (analog)	B-PD	B-PD	B-PD	B-PD	B-PD

- B-PD stands for Bulk or PDSOI → similar scalability.
- Different Technology Elements for different applications
- Gate stack & mobility enhancement techniques are possible options for 45nm node and beyond

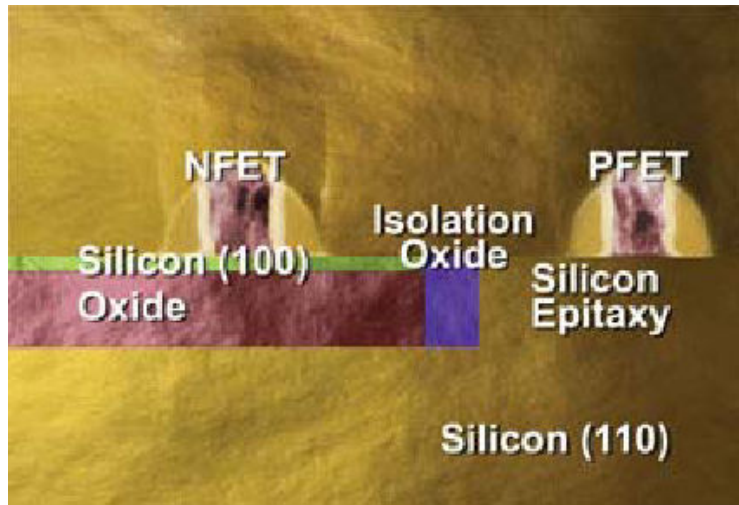
Global strain , local strain , or other techniques

	NMOS	PMOS
Biaxial Tensile Strain	↑	↑
Contact etch-stop liner (DSL)	↑	↑
SMT	↑	0
e-SiGe	0	↑
Substrate Orientation (HOT)	0	↑
Channel Orientation (<100>)	0	↑

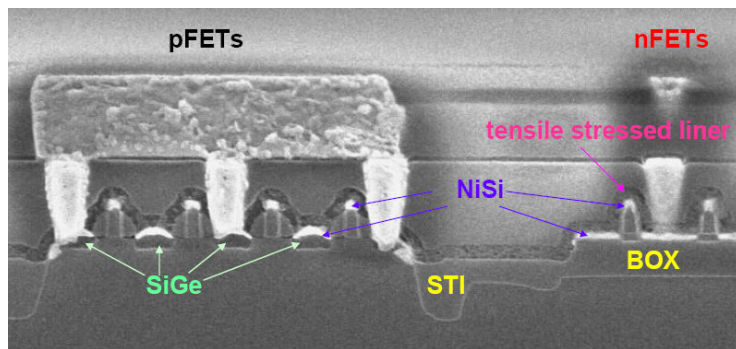
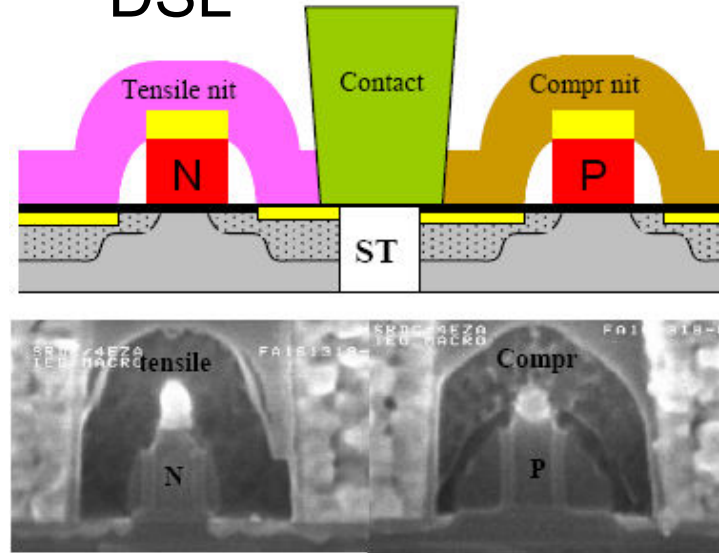
- Already in 90/65 nm nodes

Tremendous progress in mobility enhancement techniques

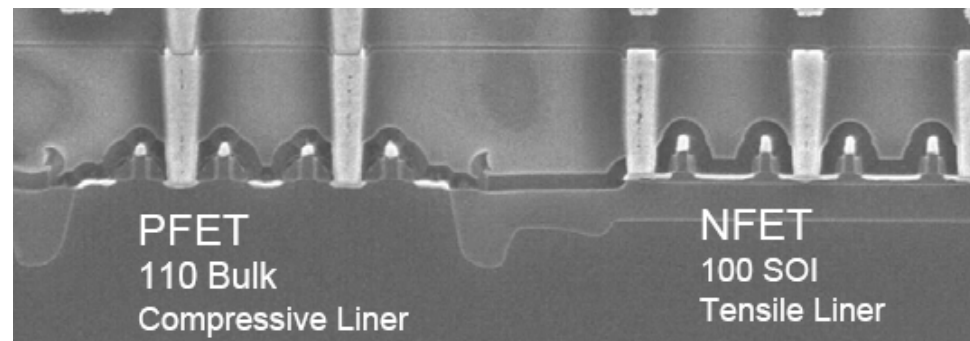
[M Yang IEDM03] H²O²



DSL [H Yang IEDM04]



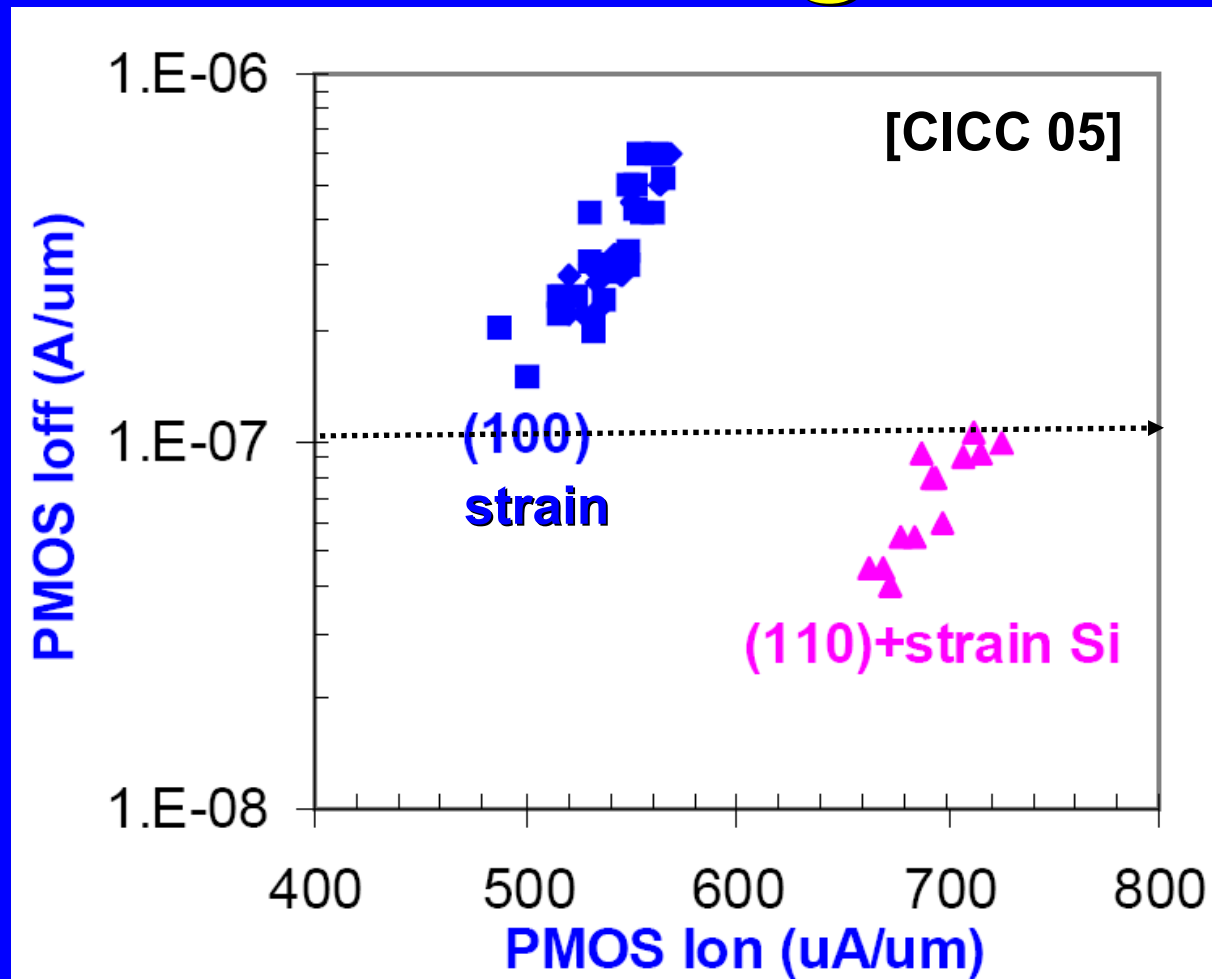
e-SiGe H²O² [Q Ouyang VLSI05]



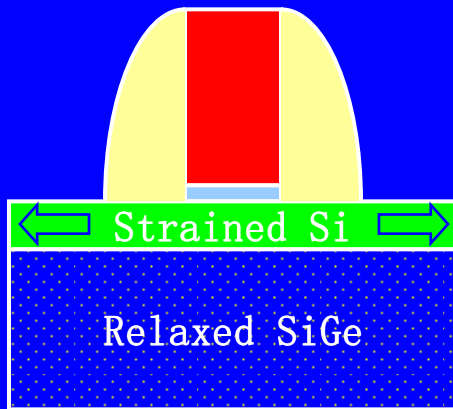
DSL H²O² [C Sheraw VLSI05]

Compressive Stress + (110) Si

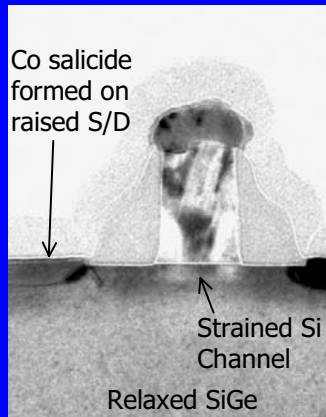
$> 700 \mu\text{A}/\mu\text{m} @ V_{\text{dd}} = 1 \text{ V}$



Biaxial Strain – Strained Silicon on Relaxed SiGe



Strained Si/SiGe Bulk MOSFET



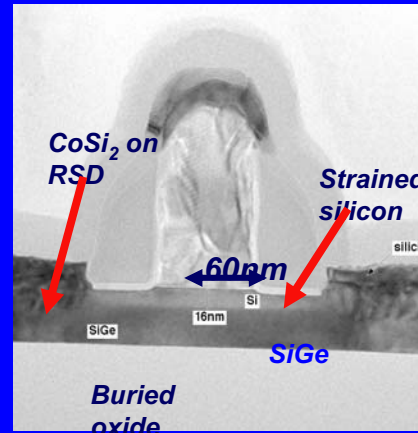
K. Rim et al., *Symp. VLSI Tech.*, p. 59, 2001.

K. Rim et al., *Symp. VLSI Tech.*, p. 98, 2002.

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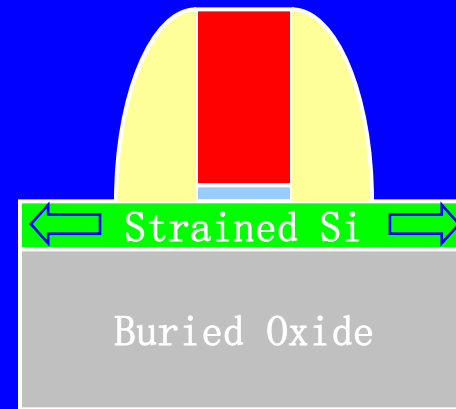


SGOI (SiGe-on-Insulator) MOSFET

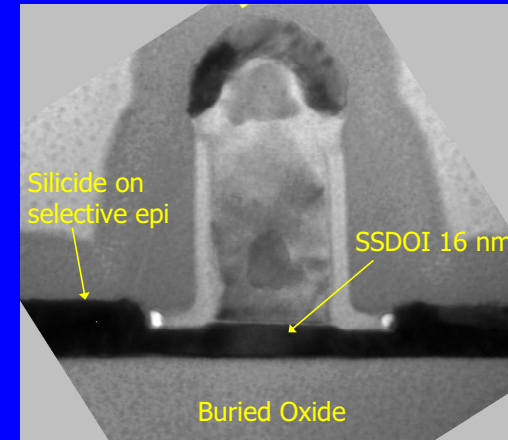


B. Lee et al., *IEDM* 2002

Meikei Jeong



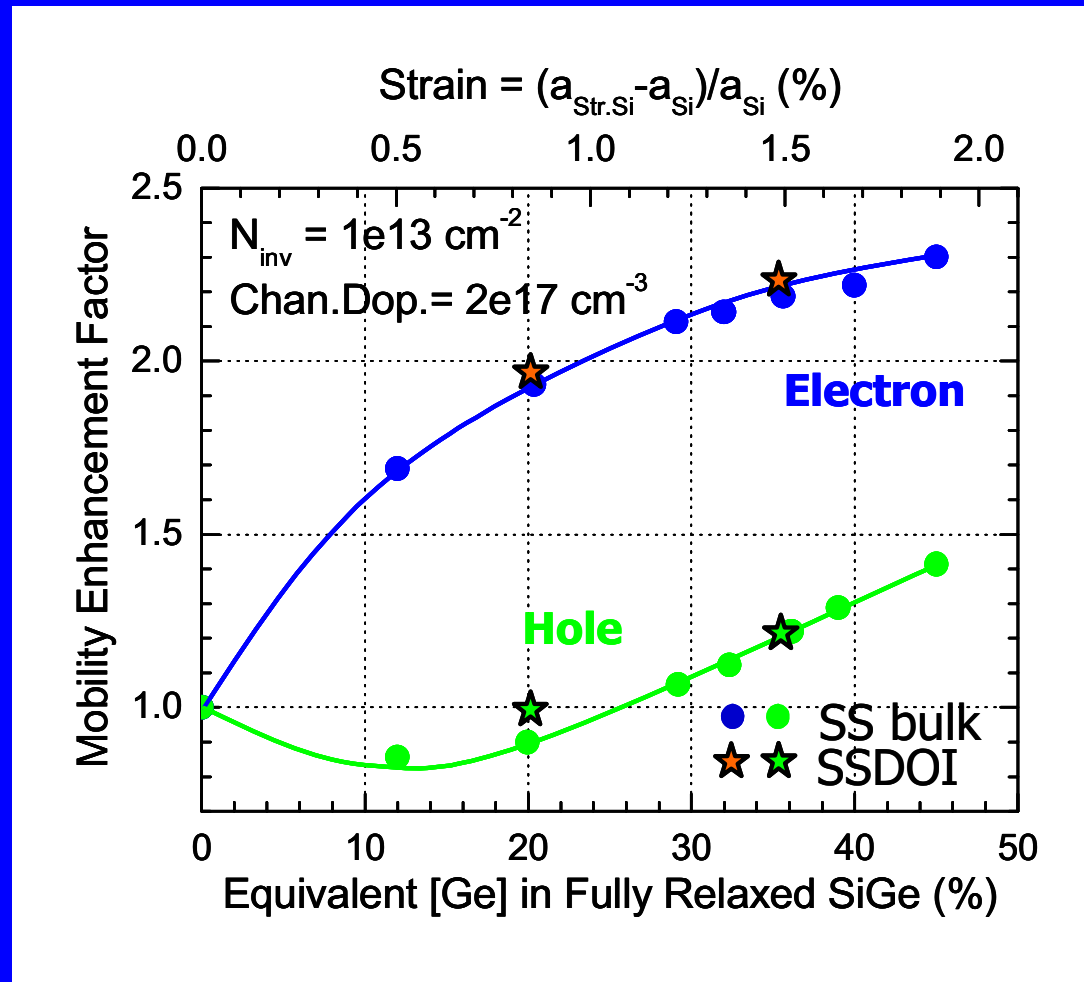
SSDOI MOSFET



K. Rim et al., *IEDM*, 2003.

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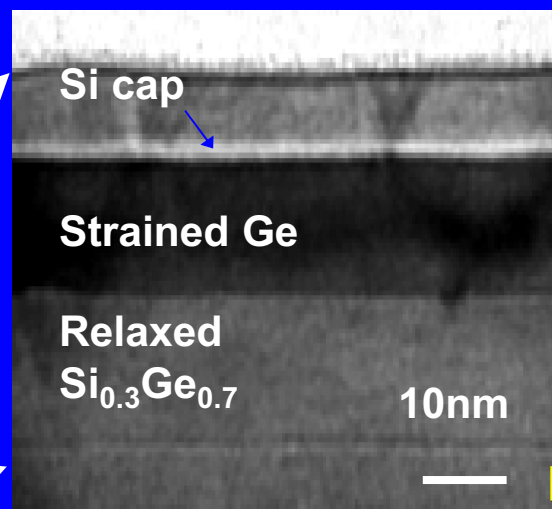
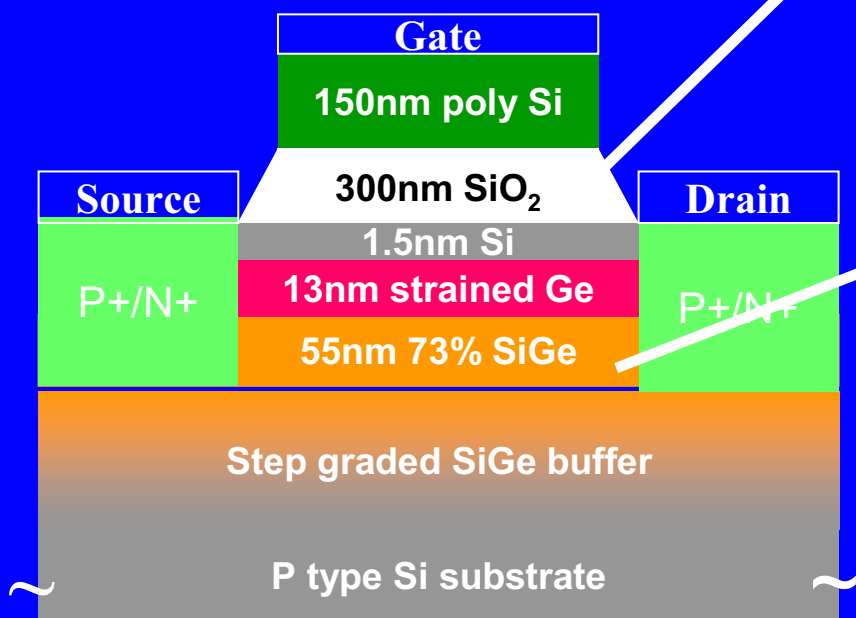
Strain-Dependence of Mobility



K. Rim et al., *IEDM*, 2003.

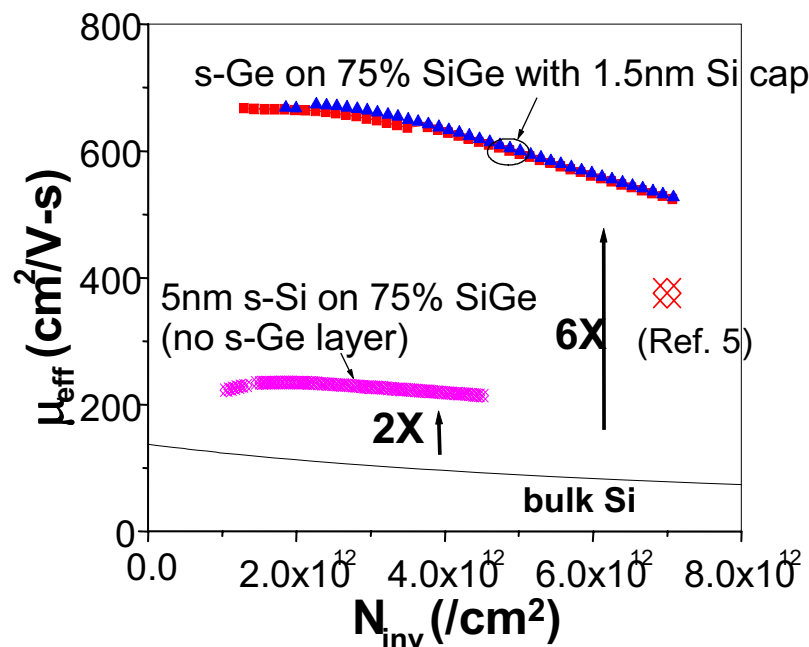
- Mobility enhancements consistent with amount of strain even for strained silicon on insulator

Strained Ge FETs



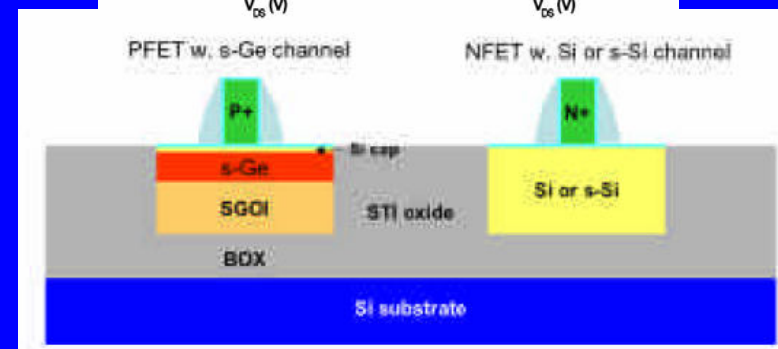
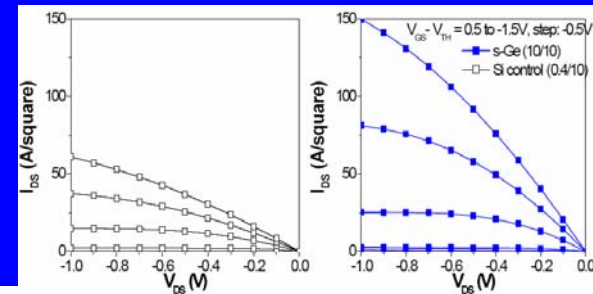
[H. Shang, VLSI04]

Much higher mobility from strained Ge:
> 2-10x higher hole mobility

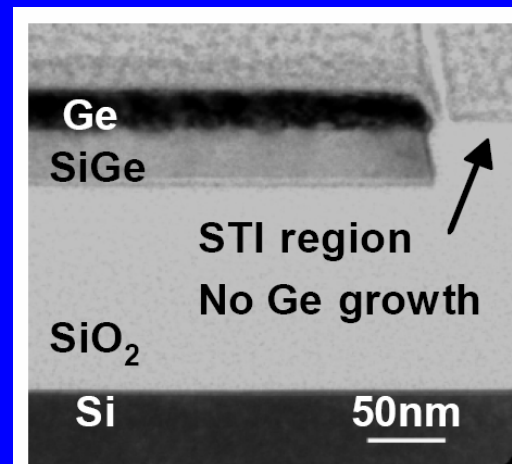


Strained Ge pFET with HfO₂

- **Integrated strained Ge on insulator with bulk Si**
 - 67% Ge by Ge condensation
 - Selective UHVCVD Ge on Si
- **3X drive current improvement**



- (1) Start with SOI or SGOI wafers
- (2) Perform standard STI isolation
- (3) Cover NFET region with oxide or nitride
- (4A) Grow Ge layer by selective UHVCVD
- (4B) Enrich Ge content by local thermal mixing
- (5) Strip the oxide/nitride cap from NFET regions
- (6) Complete standard CMOS integration: Gate stack, implant and metal contact



H. Shang, J. O. Chu, S. Bedell, E. P. Gusev, P. Jamison, Y. Zhang, J. A. Ott, M. Copel, D. Sadana, K. W. Guarini, and M. Ieong, "Selectively formed high mobility strained Ge PMOSFETs for high performance CMOS," *IEDM Tech. Dig.*, pp. 157-160, December 2004.

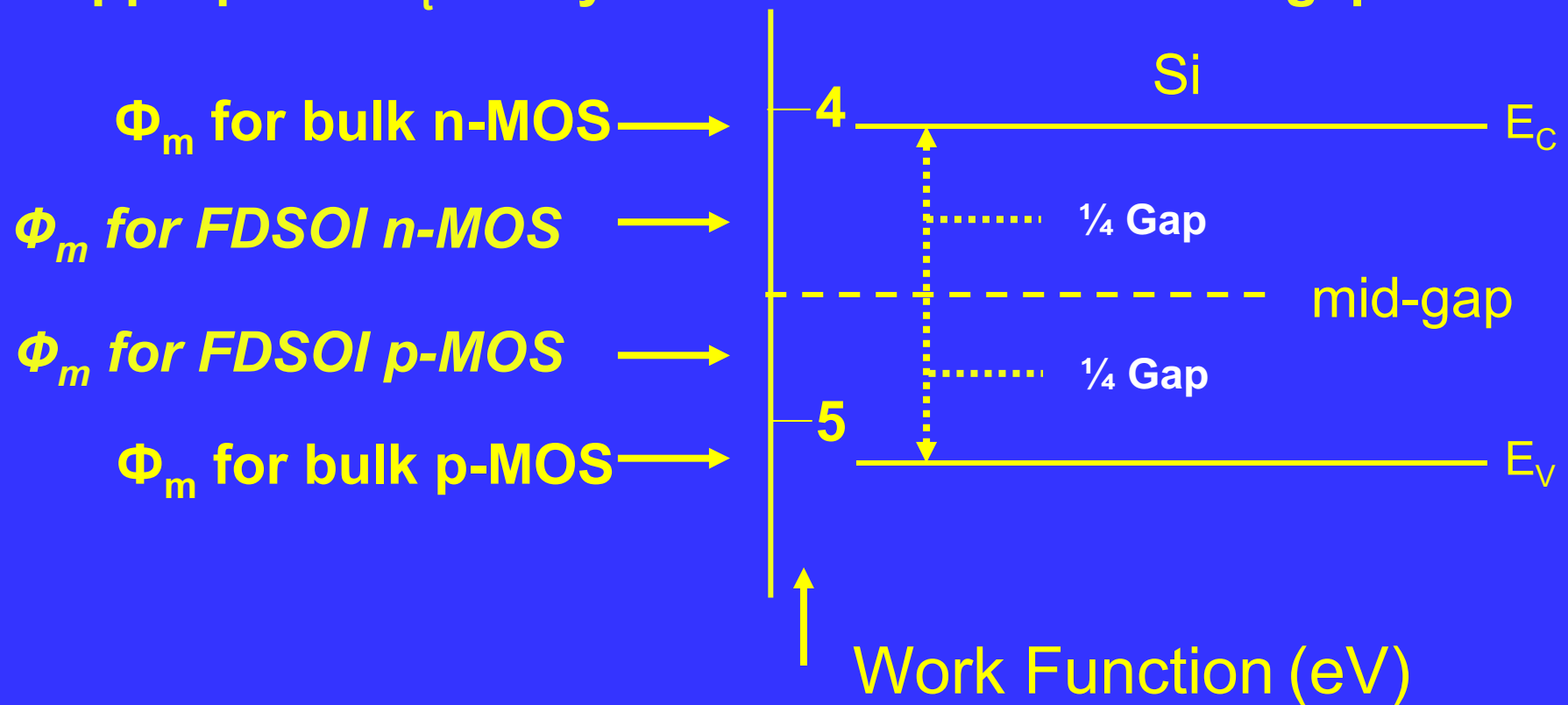
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Metal Gate Work-Function Requirements

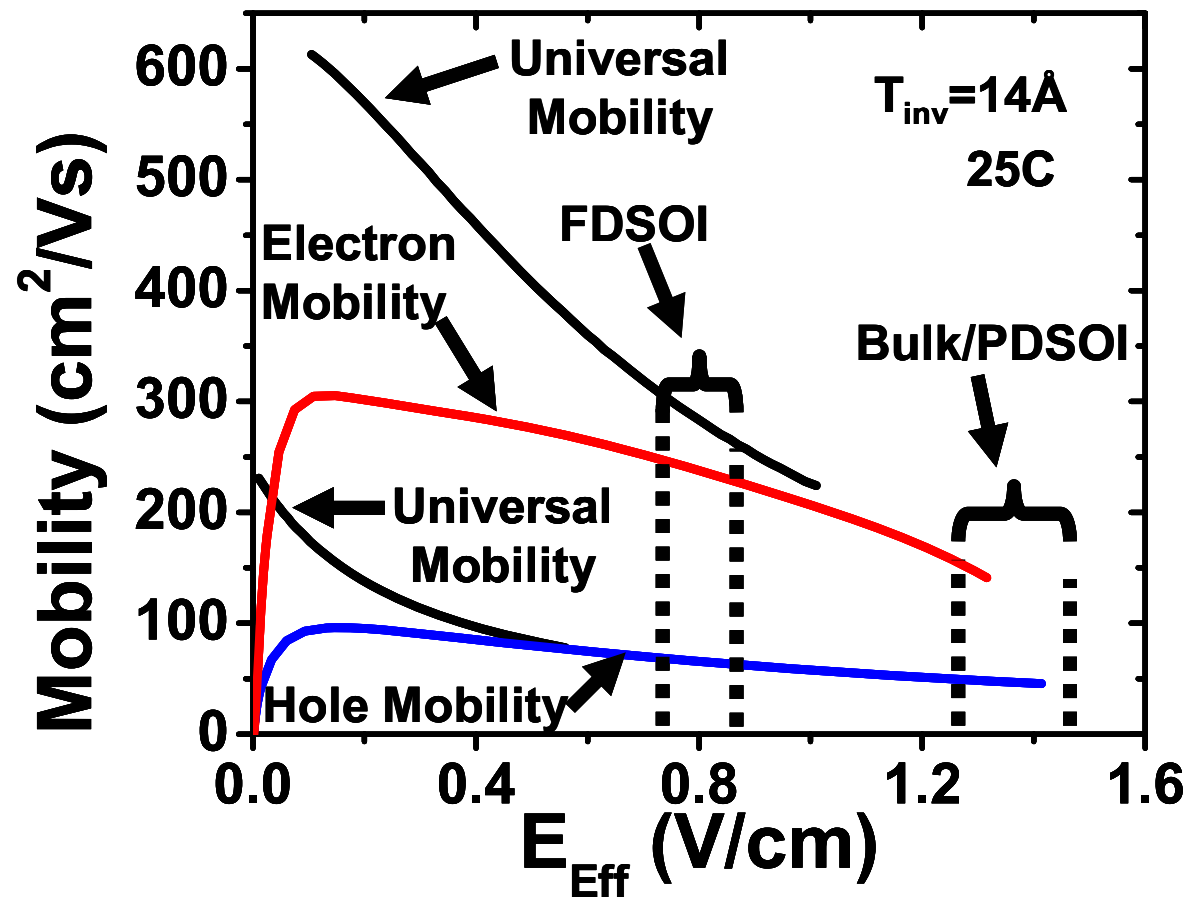
- Band-edge metals needed for Bulk/PDSOI
- FDSOI has less demanding requirement on metal work-function.
- Since T_{Si} is controlling SCE less halo is needed.
- Appropriate V_t 's may be achieved with near $\frac{1}{4}$ gap metals.



Bulk vs. Planar SOI

- Bulk and PDSOI → similar scalability.
- Opportunity for FDSOI:
 - Better scalability
 - Lower/no channel doping
 - Lower operating field
 - More options for gate conductor

Mobility



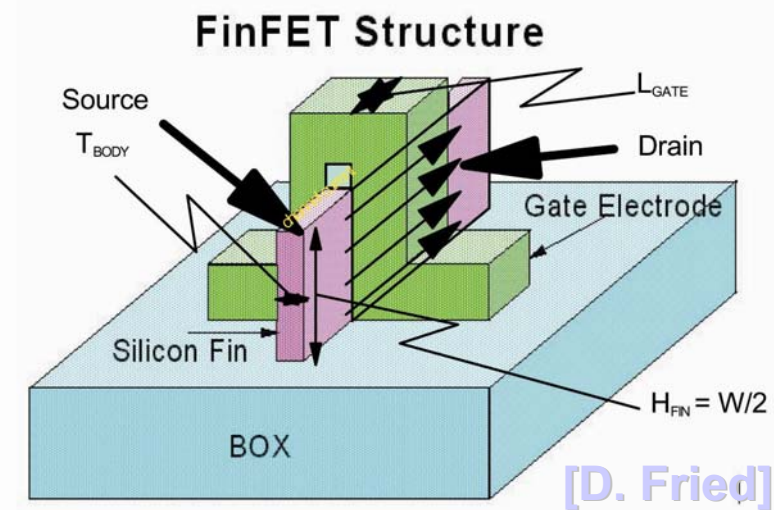
Summary MG/UTSOI

[B Doris, VLSI05]

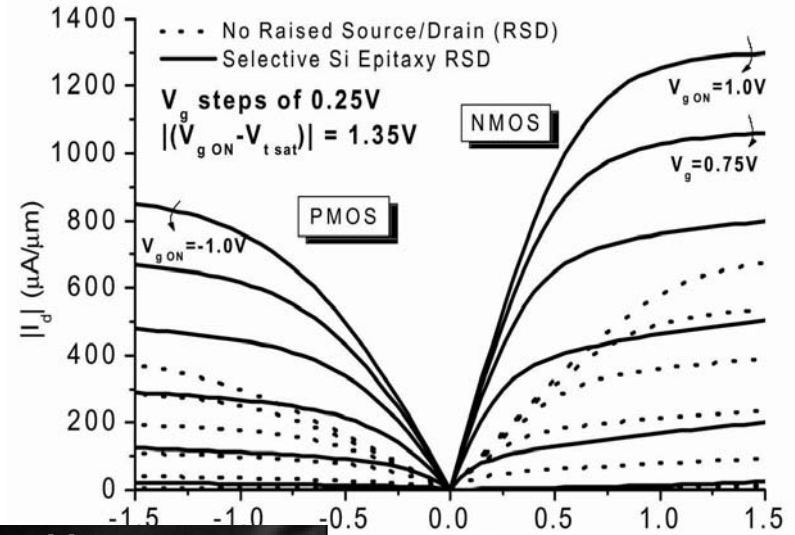
	This Work	Ref. [5] Bulk	Ref. [7] FDSOI
pFET $I_{on}(\mu A/\mu m)/I_{off}$ (nA/ μm) (1.3V)	770 28	710 45	325 0.02*
nFET $I_{on}(\mu A/\mu m)/I_{off}$ (nA/ μm) (1.3V)	1050 90	1660 46	520 10*
L gate (nm)	50	80	60
Electron Mobility (cm ² /Vs) at $E_{eff}=1MV/cm$	207	190	NA
T_{inv} (Å)	14.0	14.5	29
CV/I pFET (ps)	2.08	3.49	2.86
CV/I nFET (ps)	1.53	1.55	1.79

Finfet vs Tri-gate

FinFET: from Devices to Circuits

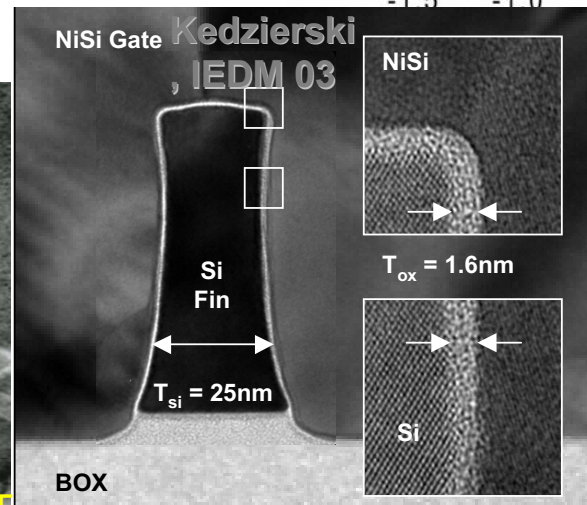
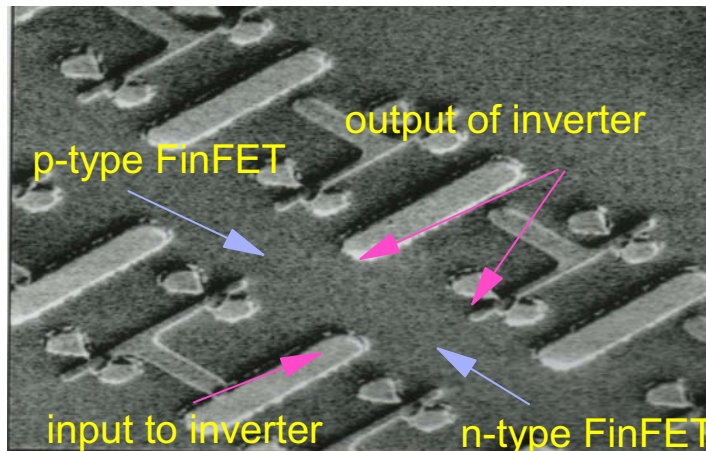


Kedzierski, IEDM 02

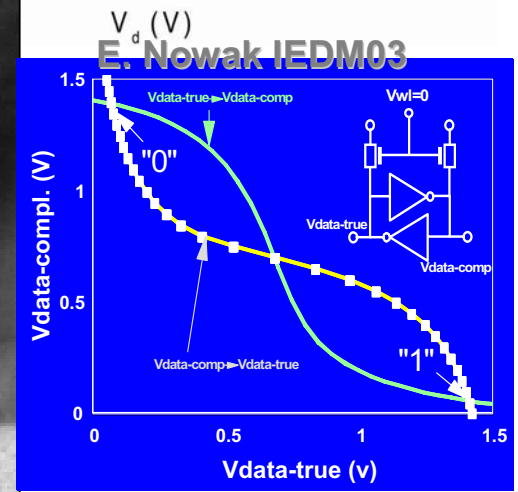


[B Rainey et al, DRC 2002]

Plan view SEM

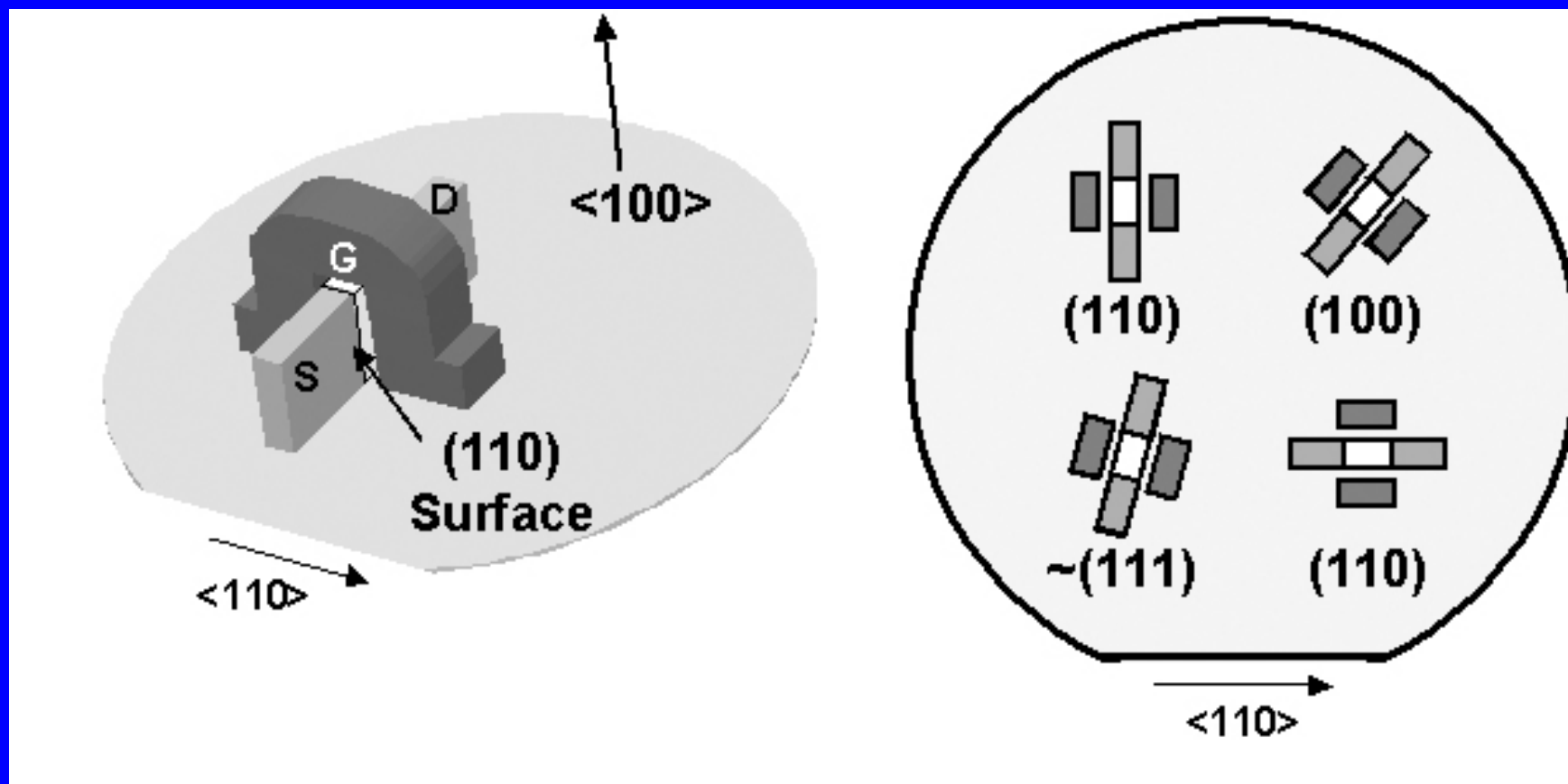


Kedzierski, IEDM 03

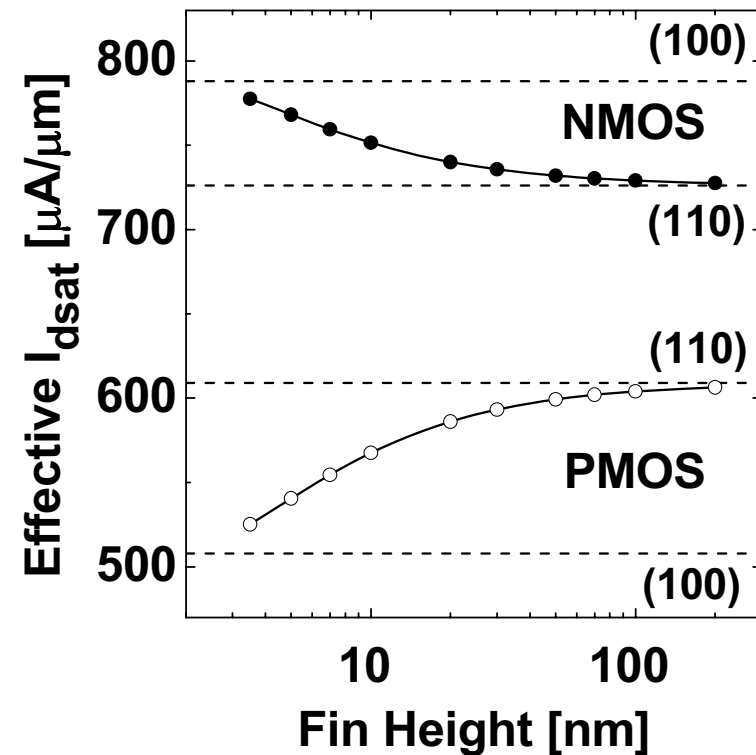
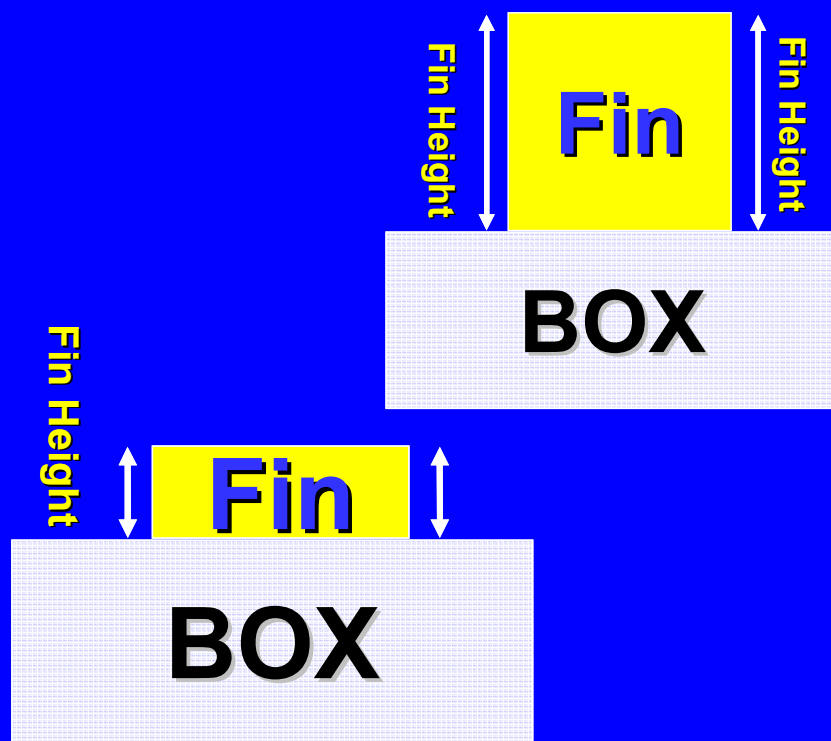


E. Nowak IEDM03

Channel Surface Orientation is Layout Dependent in FinFET



Triple-gate Structure



**Triple-gate Structure:
How to fully optimize both NMOS and PMOS
drive currents simultaneously ?**

For High - performance or low - power applications ?

- B-PD stands for Bulk or PDSOI → similar scalability.
- Different Technology Elements for different applications
- Integration is the key

Technology	65nm node 2006-07?	45nm node 2008-10?	32nm node 2010-13?	22nm node 2012-16?	15nm node 2014-19?
High performance (HP)	B-PD	B-PD	FD/Fin	FD/Fin	FD/Fin
Low operating power (LOP)	B-PD	B-PD	FD/Fin	FD/Fin	FD/Fin
Low standby power (LSTP)	B-PD	B-PD	B-PD	FD Fin	FD/Fin
Other (analog)	B-PD	B-PD	B-PD	B-PD	B-PD

Si nanowire , carbon nanotube FET , or other new devices , and when ?

- not likely to challenge any previous mentioned options for 32nm node

32nm Options: Q&A

- Bulk or planar SOI , and when ?
 - FDSOI
- FinFET or tri - gate , and when ?
 - FinFET
- - Global strain , local strain , or other techniques , and when ?
 - NFET: Global, PFET: HOT+STRAIN
- - For High - performance or low - power applications ?
 - Co-exists
- - Si nanowire , carbon nanotube FET , or other new devices , and when ?
 - Not likely