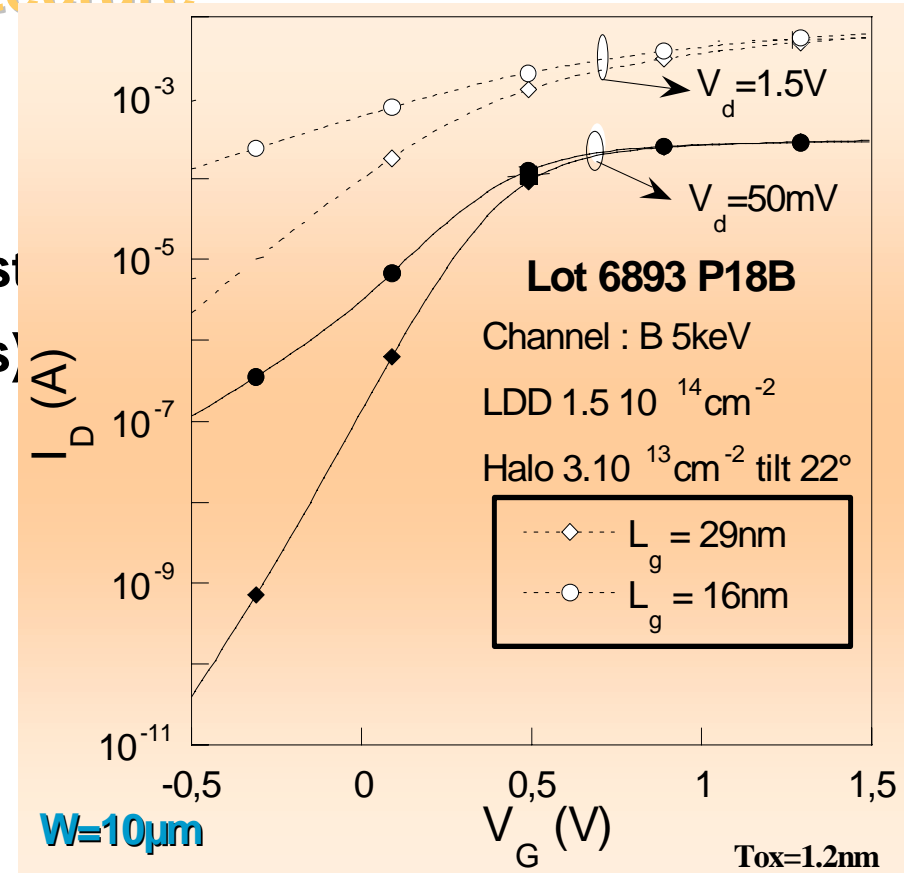


Nanoscale MOSFET fabrication

Bulk: improvement with superhalo

Conventional MOSFET architecture

- 1.2nm SiO₂ gate oxide
- In situ doped polysilicon Gate
- Channel : non intentionnaly adjust
but Super Halo SH :(only BF₂ halos)
or Non super Halo NSH :
(B II + BF₂ halos)
- As extensions
- 30nm nitride spacers
- As HDD Source and drain
- RTP spike anneal 1050°C



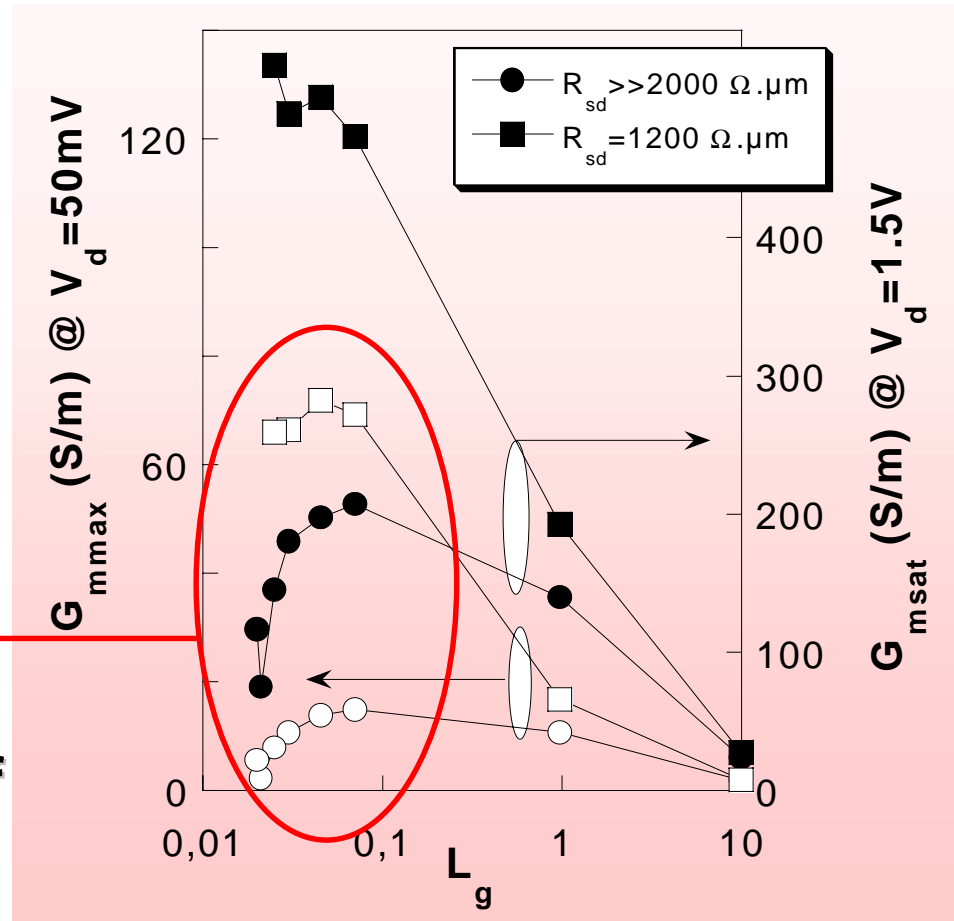
L_{gmin} = 16nm

G. Bertrand et al., Proceedings
ULIS 2003
SSE July 2004

Limitation to transport

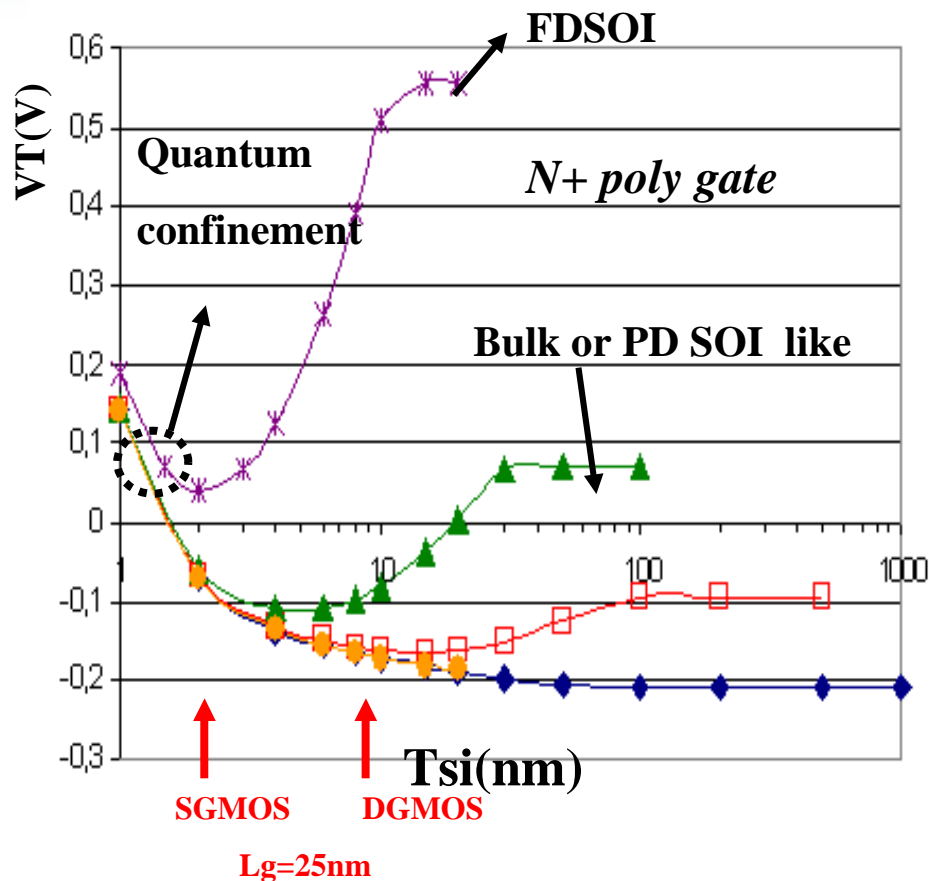
- Impact at room temperature

Low field mobility degradation due to halo overlap mostly in the case of efficient SCE control



G. Bertrand et al., Proceedings
ULIS 2003
SSE July 2004

From Fully Depleted SOI to Double Gate CMOS



Fully depleted SOI:
$$V_{T1} = V_{fb1} + 2\phi_f + \frac{qN_A T_{si}}{2C_{ox1}}$$

Quantum confinement:

$$E_n^\infty = \frac{\pi^2 \hbar^2}{2m_e} \times \left[\frac{n}{T_{si}} \right]^2$$

Low Doped thin channel

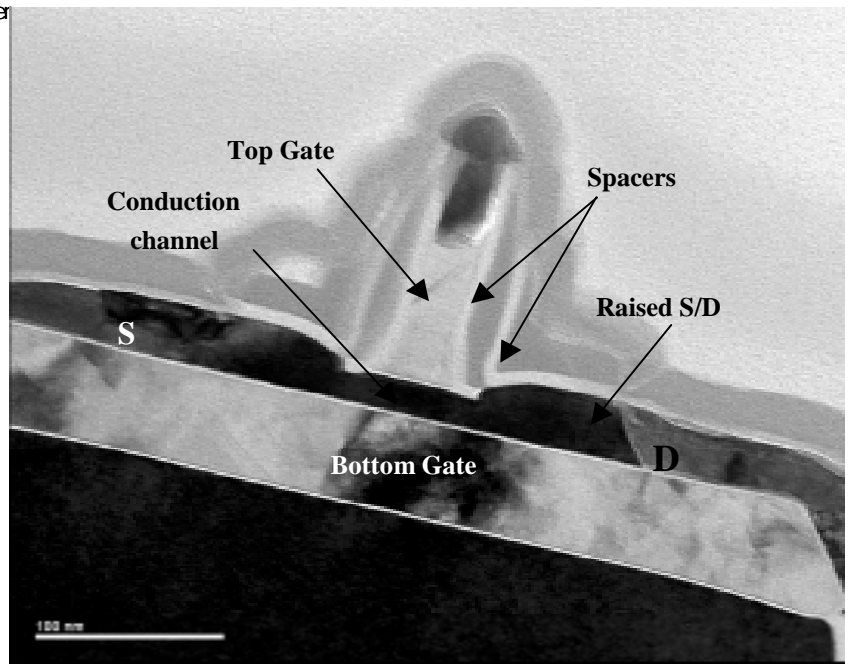
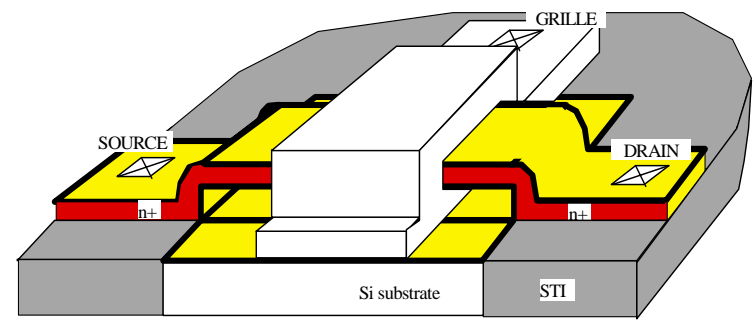
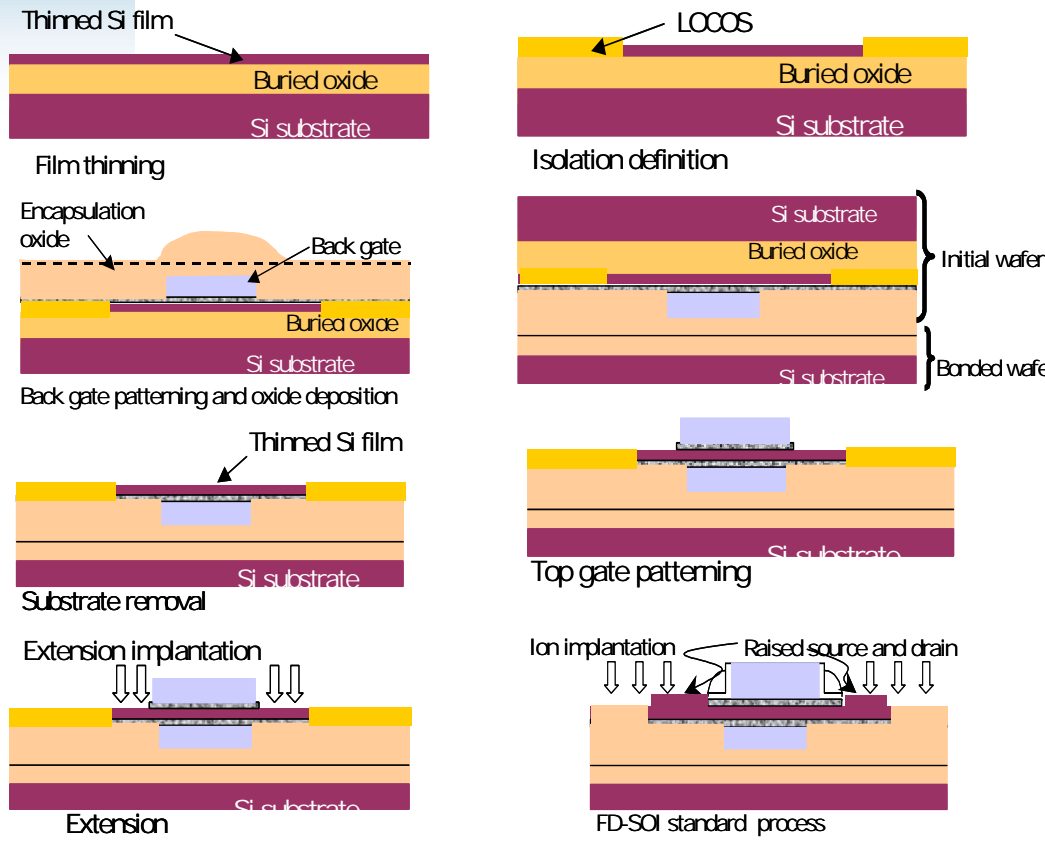
=> Lower dopant fluctuations

=> Higher V_T stability vs thickness

J.Lolivier et al,
ECS Spring meeting, Paris May 2003

Gate Workfunction engineering for
dual gate /undoped FD channel Low VDD

Multigate MOSFET architectures : the Planar approach

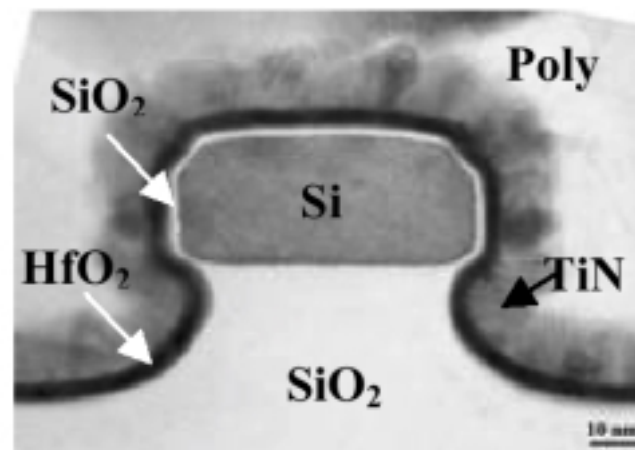
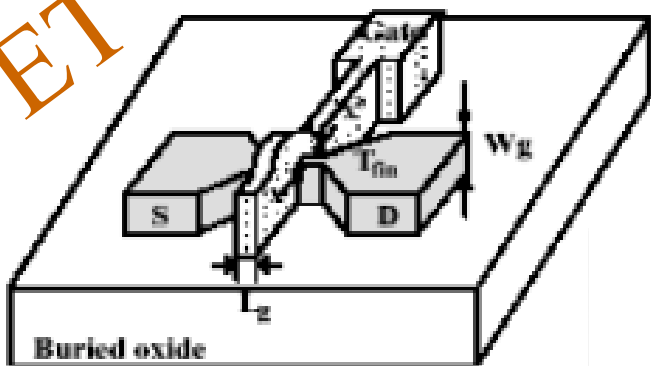


LETI: Wafer Bonding TiN gate
M. Vinet et al., SSDM2004, Sept 2004

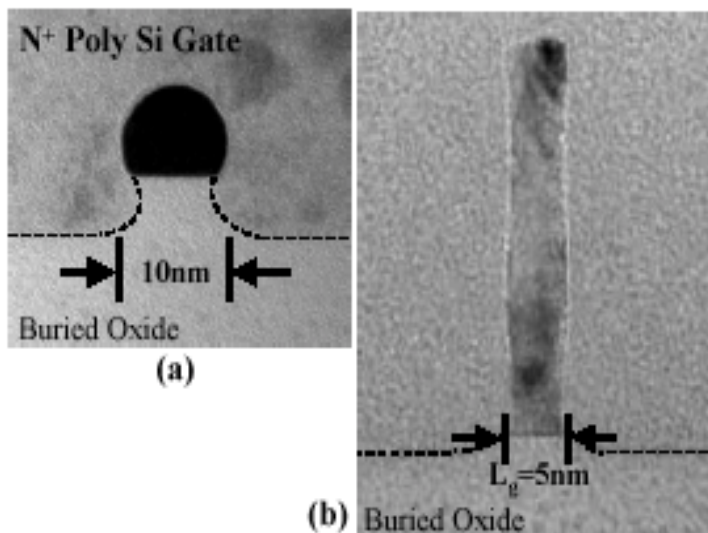
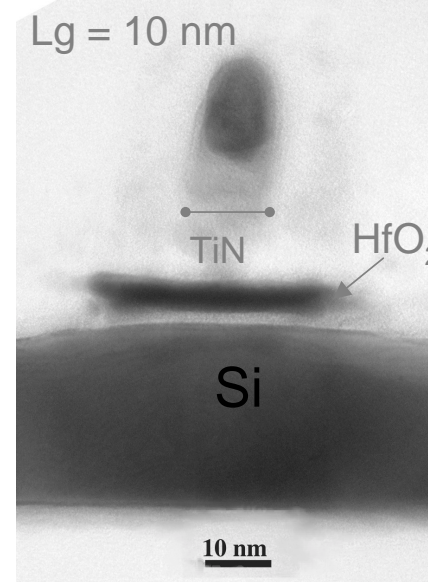
STMicroelectronics : SON GAA Lg=25nm
S.Harrison et al., SN Workshop 2004,
S.Monfray et al. ,IEDM2004

Multigate MOSFET architectures : Non Planar approach

FinFET

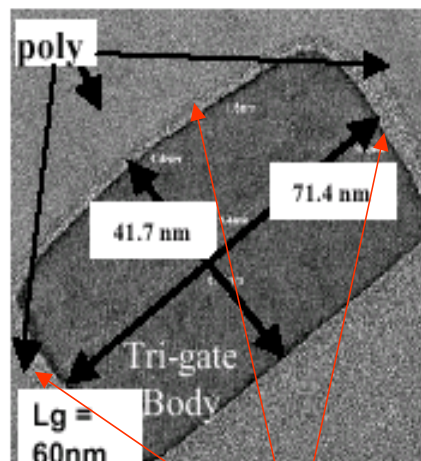


C. Jahan et al., VLSI Tech Symp 2005, Ω FET $L_g=10\text{nm}$ TiN/HfO₂ gate stack



TSMC: Poly gate FinFET $L_g=5\text{nm}$

FLYang et al., VLSI Tech Symp 2004



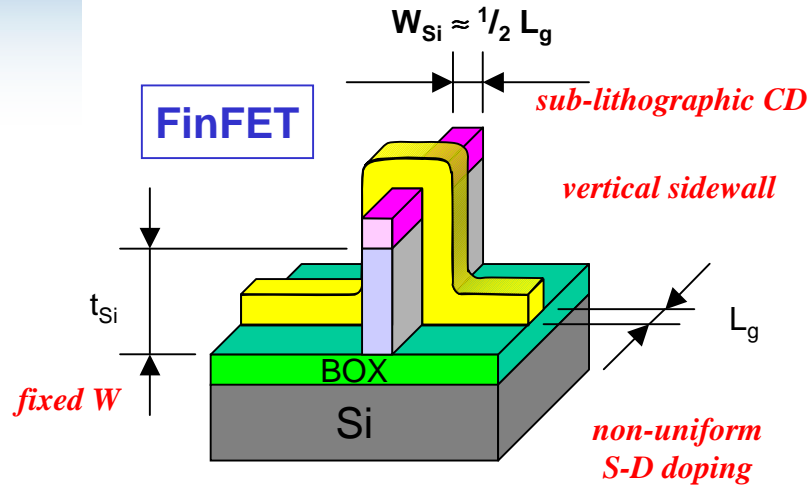
3 channels

INTEL: Poly gate Trigate $L_g=60\text{nm}$

B. Doyle et al., VLSI Tech Symp 2003

Scaling capabilities

From FDSOI to DG/FinFET via Trigate



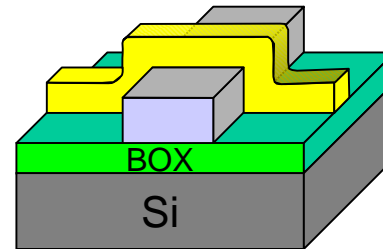
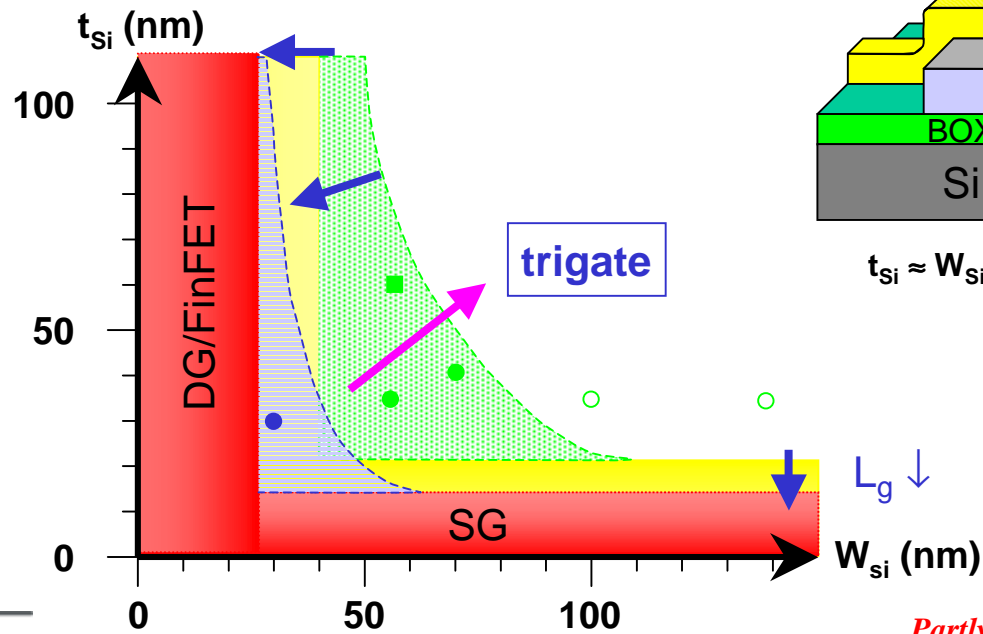
- t_{Si} remains \approx thickness SOI manufact. specs
 \Rightarrow transfer W_{Si} control

-Design rules & layout issues
 (compatibility with existing design libraries):

$$W_{FETmin} = 2 * t_{Si} + W_{Si}$$

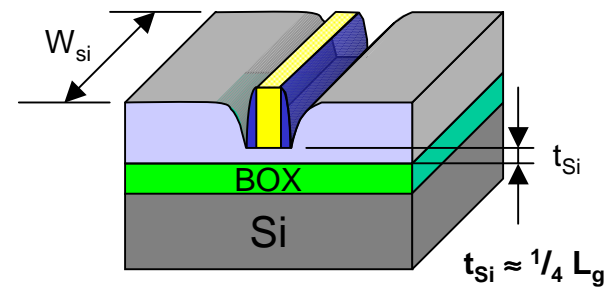
$$W_{FET} = n * W_{FETmin}$$

\Rightarrow layout factor ($W_{FETmin} / \text{pitch}$)



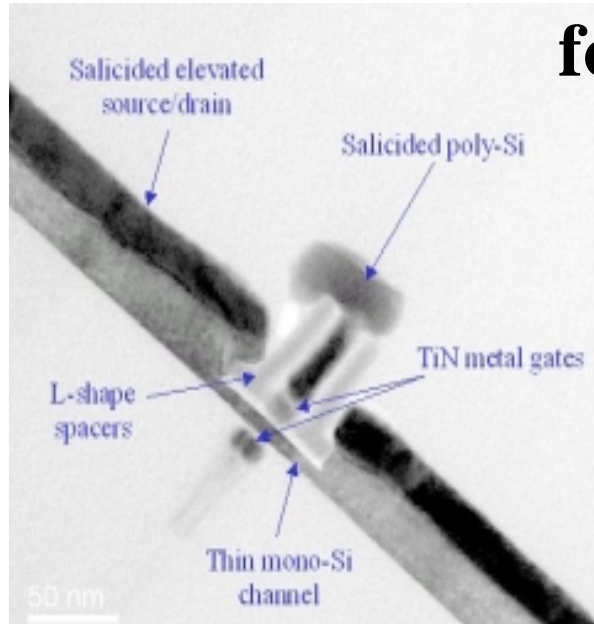
Best of both worlds?

FD-SOI

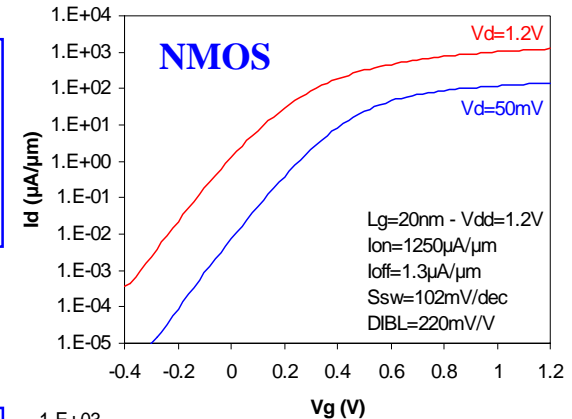


Partly from B.Doyle et al, VLSI2003 paper 10A-2, Kyoto(Japan)

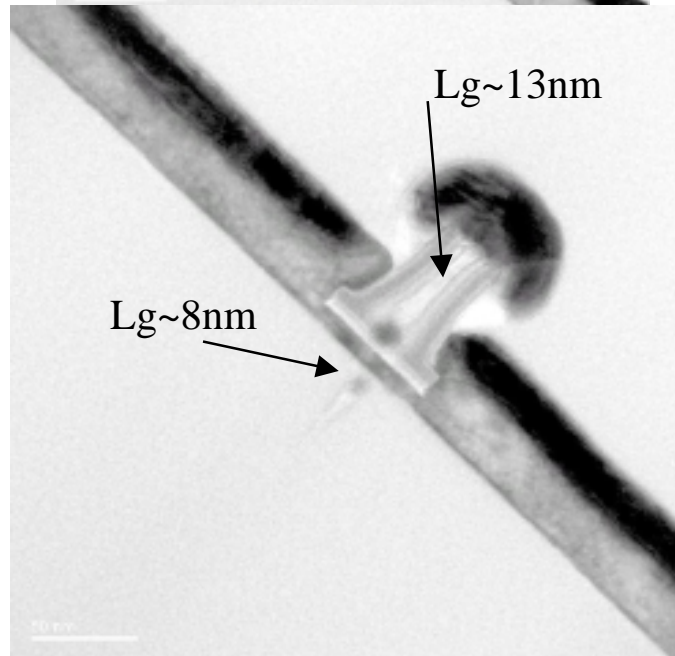
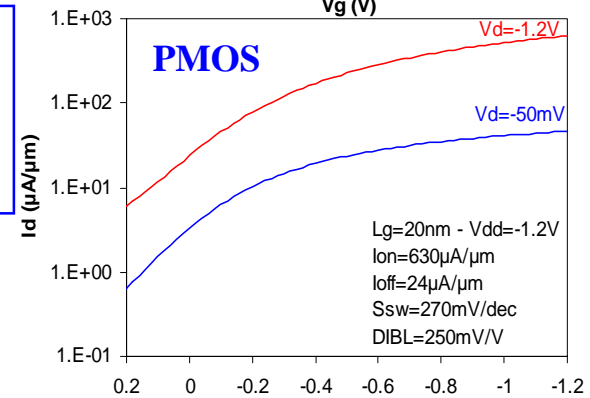
Planar Bonded double metal gate down to $L_g=10\text{nm}$ for High Performance



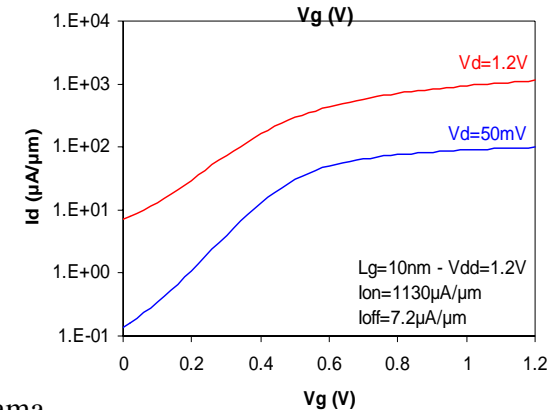
$L_g=20\text{nm}$
 $I_{on}=1250\mu\text{A}/\mu\text{m}$
 $I_{off}=1.3\mu\text{A}/\mu\text{m}$
 $T_{si}\sim 10\text{nm}$



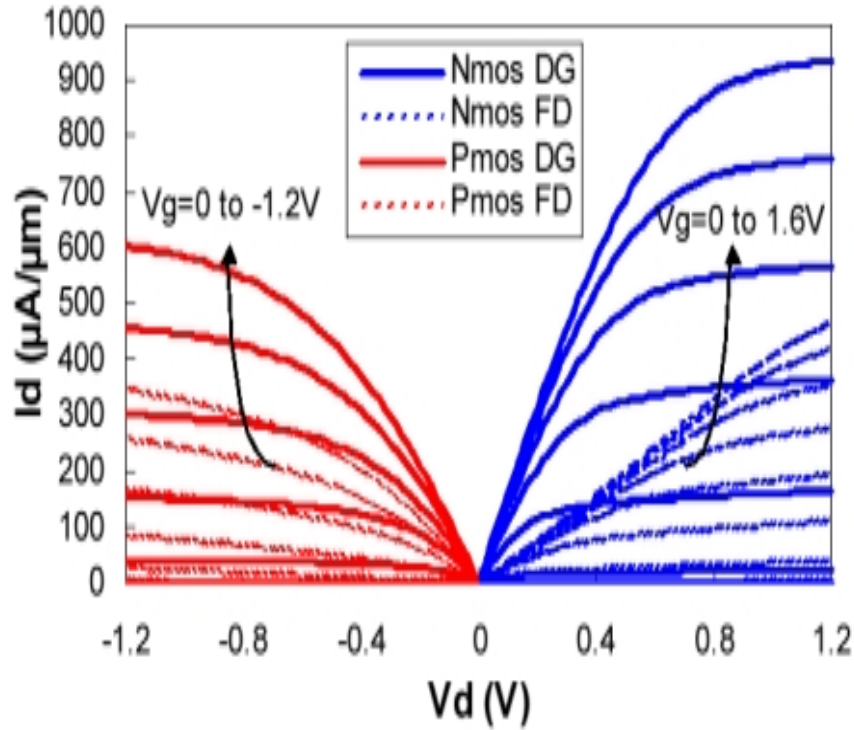
$L_g=20\text{nm}$
 $I_{on}=630\mu\text{A}/\mu\text{m}$
 $I_{off}=24\mu\text{A}/\mu\text{m}$
 $T_{si}\sim 7\text{nm}$



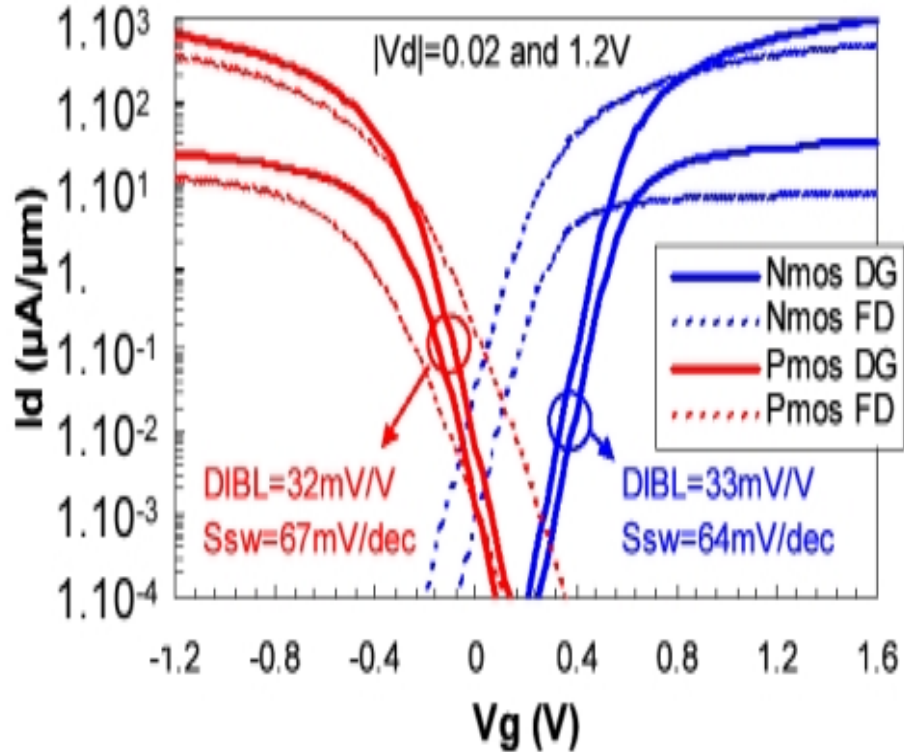
$L_g=10\text{nm}$
 $I_{on}=1130\mu\text{A}/\mu\text{m}$
 $I_{off}=7.2\mu\text{A}/\mu\text{m}$
 $T_{si}\sim 6\text{nm}$



Double gate versus Single gate(FDSOI) MOSFET by Wafer Bonding(Lg=40nm)



Output characteristics of 40nm drawn gate length DG and FD transistors.



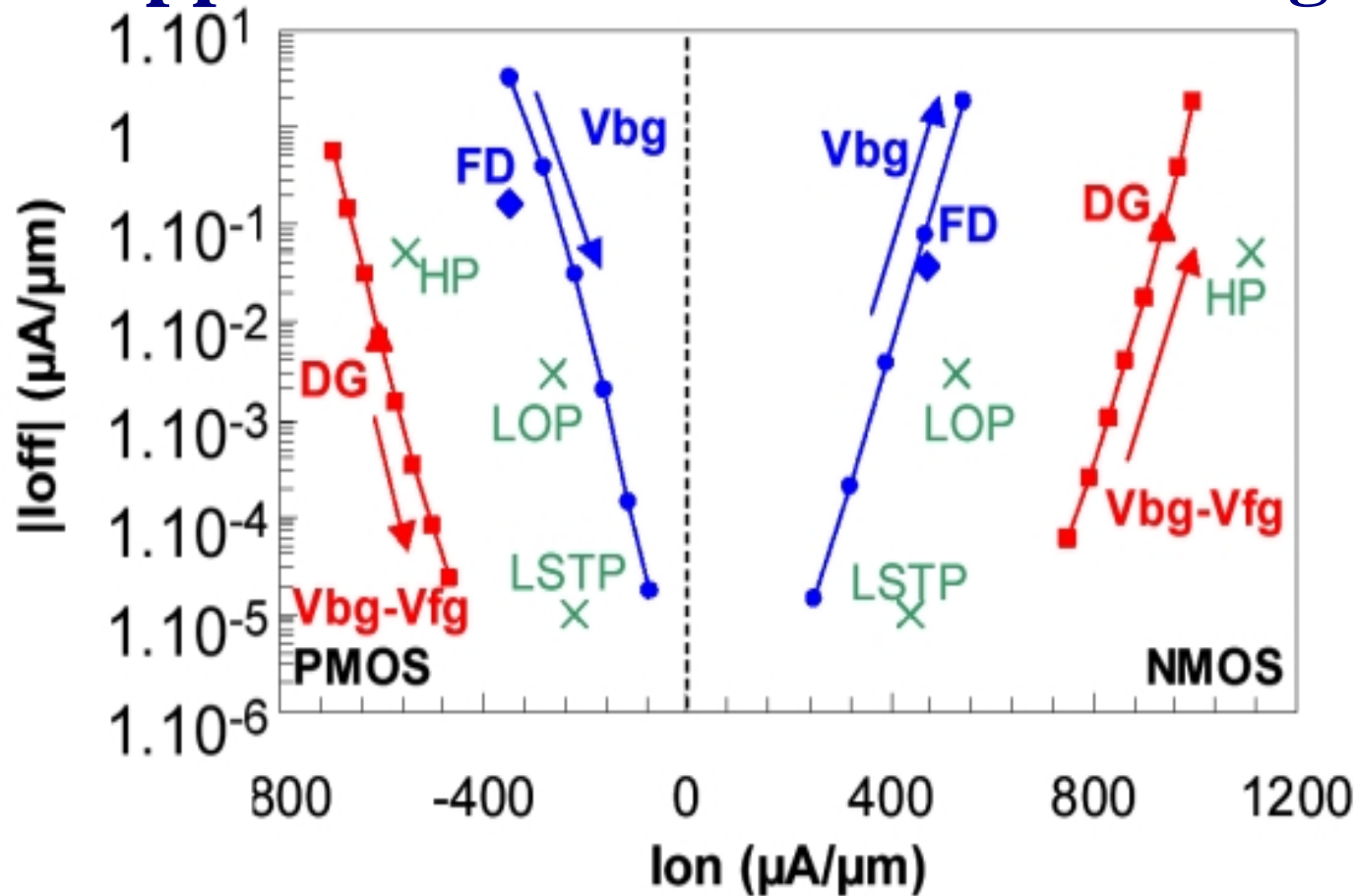
Transfer characteristics of 40nm drawn gate length DG and FD transistors @ $V_d=20mV$ and $1.2V$

M.Vinet et al. , SSDM 2004, Sept2004, Tokyo

IST NESTOR project



Multigate devices for Multipurposes applications for Future SOC designs

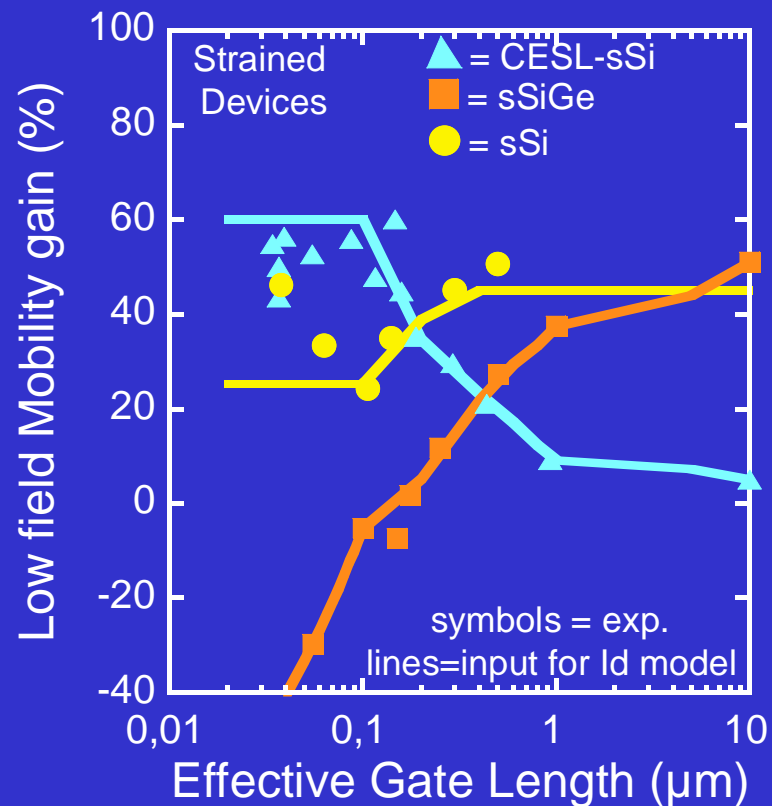


Double gate MOSFET by bonding

I_{off} vs I_{on} of tunable DG MOS (adjustable V_{bg}-V_{fg}) and tunable DG MOS operating in FD mode (adjustable V_{bg}) between Low-stand-by-power (LSTP) and High-performance (HP) -90 nm node

M.Vinet et al. , SSDM 2004, Sept 2004, Tokyo

Mobility enhancement



- ESL-sSi : \oplus m^* reduction \oplus strain enhancement
- sSiGe : \oplus m^* reduction \ominus extra charged defects
- sSi : \ominus quantization effects \ominus phonon scattering not dominant

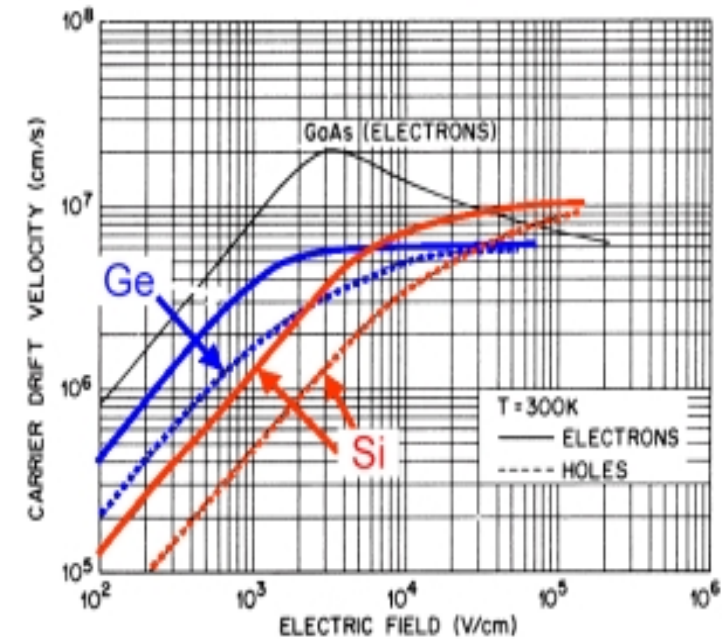
Original & in-depth characterisation of μ_{eff} in strained devices

Ge versus Si

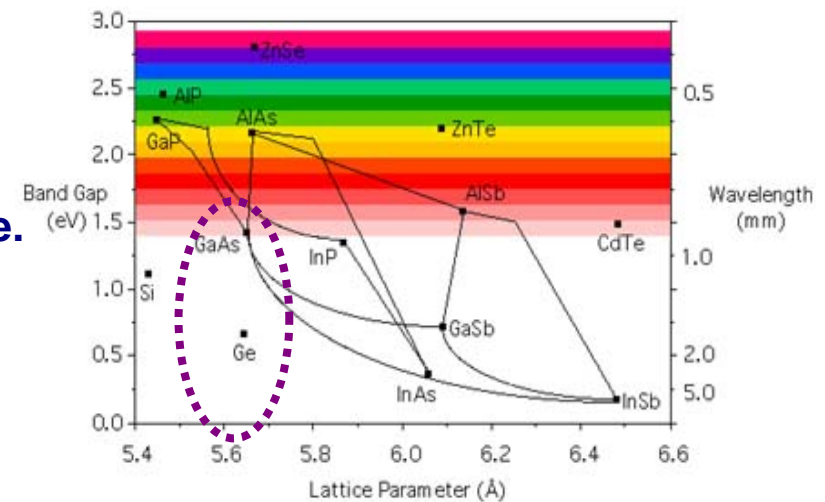
- 4 Low field mobility higher than in silicon
- 4 Electron and hole mobility values are closer than in Si => Design compactness.
- 4 Energy relaxation time > in Si=> velocity overshoot appears for higher L than in Si.
- 4 Dopant Activation at lower temperatures. High dopant diffusivity.
- 4 Compatibility with high- κ dielectrics(necessity)
- 4 GeOI : demonstrated feasibility
- 4 III-V (GaAs)/ Ge co-integration: Optoelectronics, RF, power devices,...

but

- 4 Lower bandgap than Si. Junction leakage.
- 4 Higher K than Si(C_j , SCE, DIBL,etc...)
- 4 Lower thermal conductivity than Si(Self heating,...)
- 4 CMOS process Integration is an issue



Band Gap versus Lattice Parameter for IV, III-V, and II-VI Semiconductors



GeOI substrates : the Smart-Cut™ process

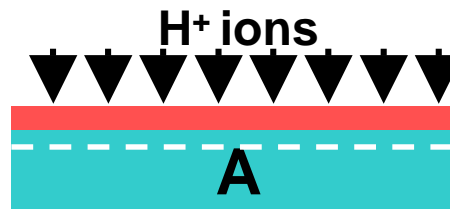
1- Donor wafer (EPI Ge/Si)



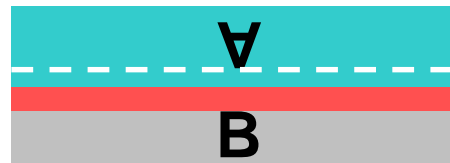
2- Oxide formation



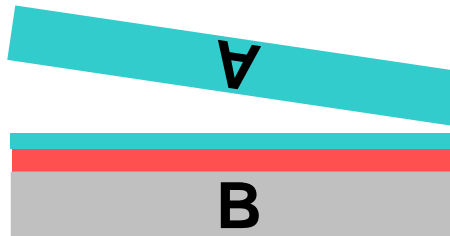
3- Implantation



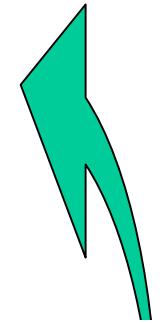
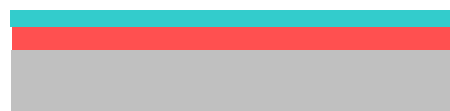
4- Cleaning / bonding



5- Layer transfer



6- Final treatments

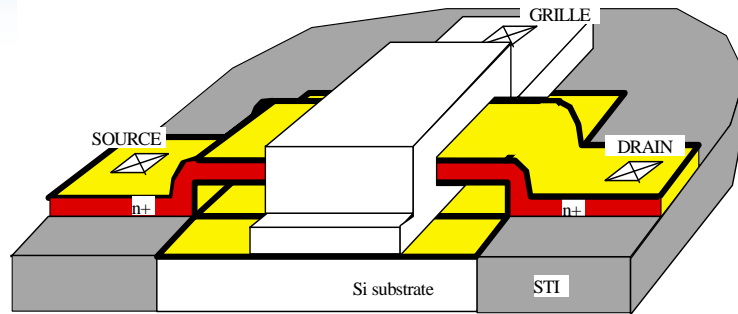


Recycling

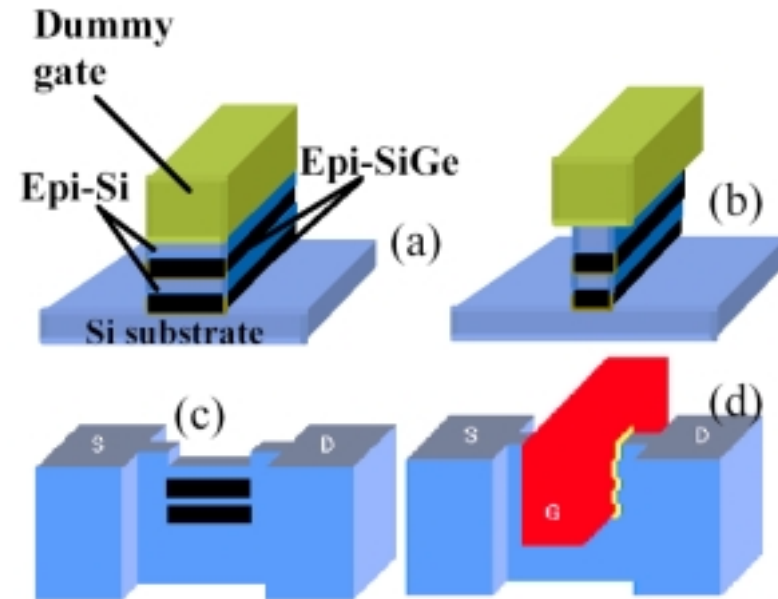


From SON to Multichannels and Multigates

Silicon On Nothing(SON)



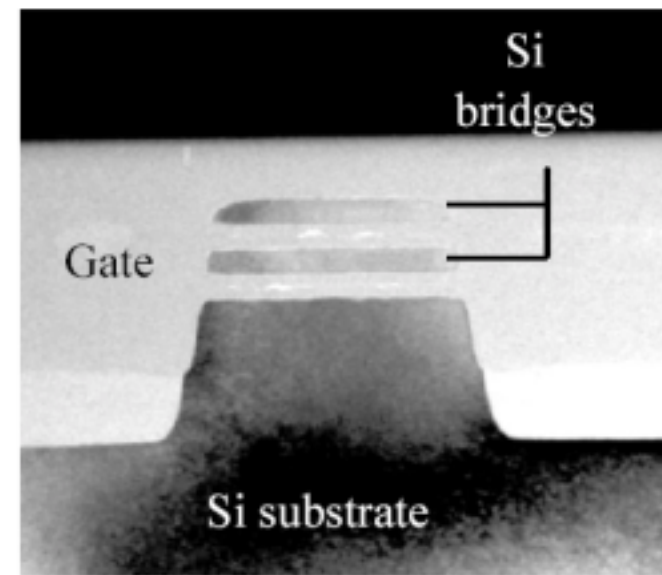
STMicroelectronics : SON GAA Lg=25nm
S.Harrison et al., SN Workshop 2004,
S.Monfray et al. ,IEDM2004



MBCFET(Multichannel)

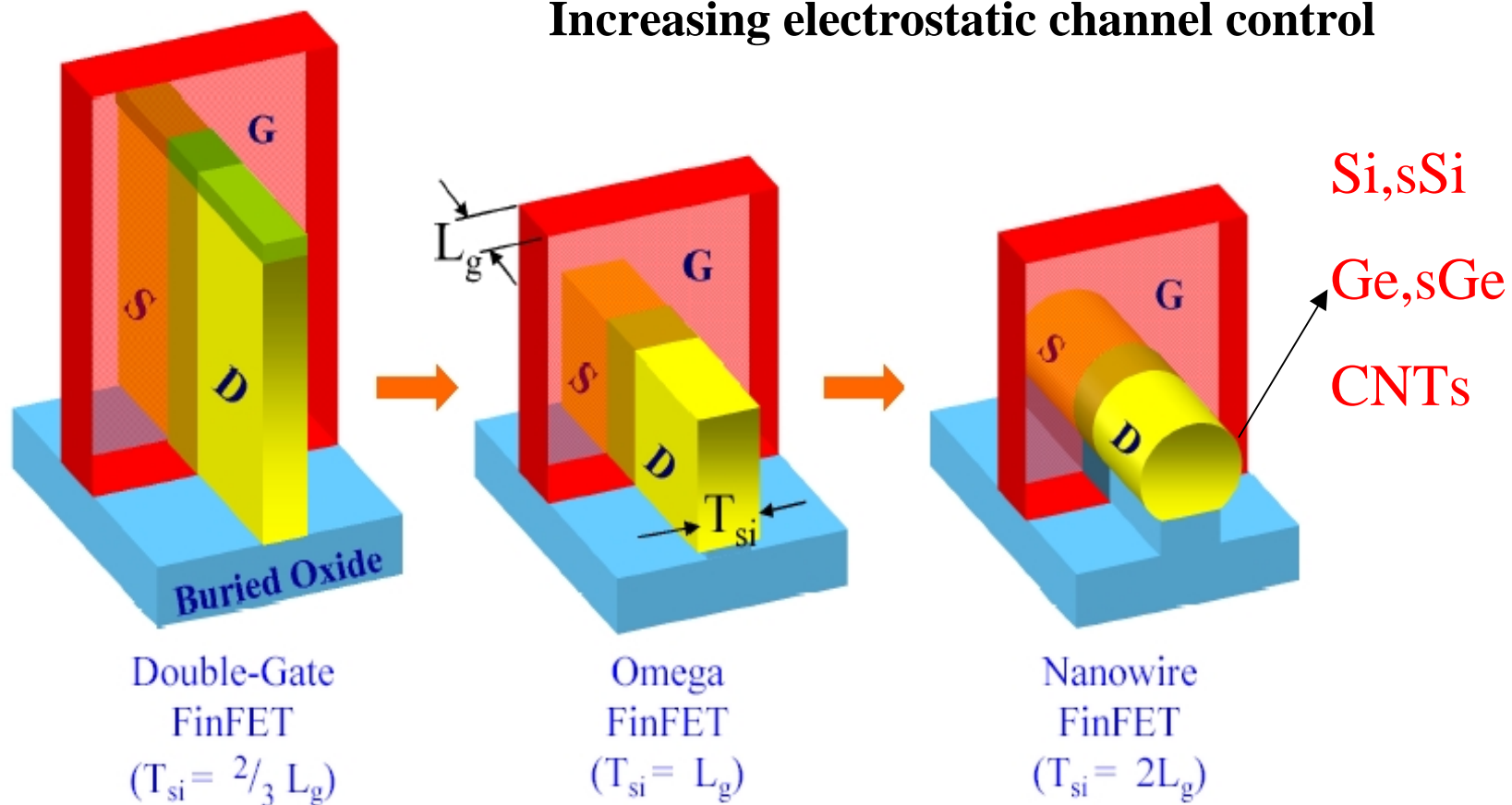
$I_{onN}=2100\mu A/\mu m$ $I_{offN}=1.3\mu A/\mu m$ $L_g=30nm$

Samsung MBCFET GAA
SYLee et al., VLSI Tech. Symp. 2004, June 2004 Honolulu(HI)
VLSI Tech. Symp. 2005, June 2005 Kyoto(Japan)



From Double gate to Nanowire

Increasing electrostatic channel control

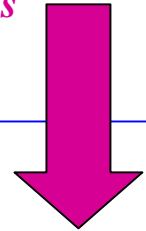


FLLiang, VLSI Tech Symposium 2004, June 2004, Honolulu(HI)



Devices architectures options

GeOI
Dual Nanowires
Multichannels
CNT

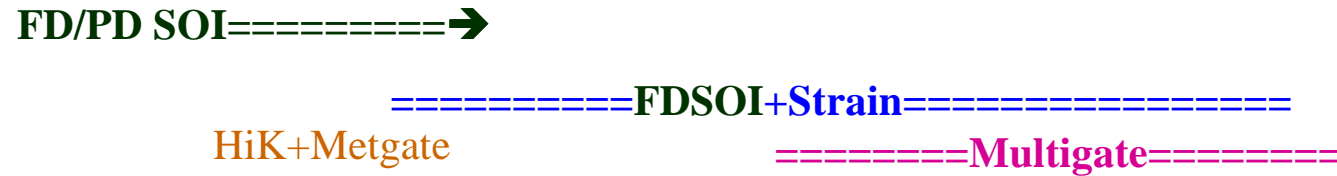


65nm	45nm	32nm	22nm
2007	2010	2013	2016

High Performance



Low Power



Low Standby Power



HP sub 32nm node(Lg=13nm ITRS)

- Bulk or planar SOI, and when?

FDSOI, introduction 2007

-FinFET or tri-gate, and when?

DGMOS Multigate 2011-2013(Lg=13nm). Co-integration with planar FDSOI.

Global strain, local strain, or other techniques, and when?

Local(2005), global and dual(otherwise impact on CMOS design)

For High-performance or low-power applications?

LSTP: FDSOI, Multigate (both w HiK + Metgate)

LOP: FDSOI+Strain, Multigate(both w HiK + Metgate)

HP: FDSOI+Strain, Multigate, Multichannels (both w HiK + Metgate)

-Si nanowire, carbon nanotube FET, or other new devices, and when?

Si, Ge, sSi, sSiGe, sGe nanowires channels On Insulator@ sub 32nm already
(Multigate w sub 10nm width) Dual channels and gates.

CNTransistors and interconnects sub 22nm node