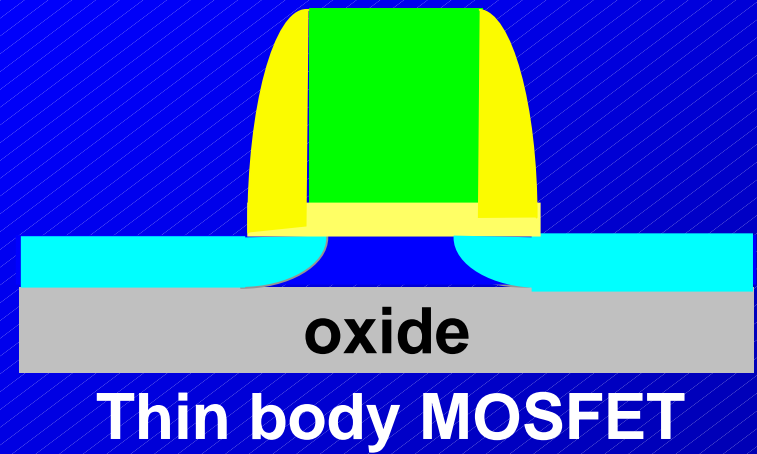
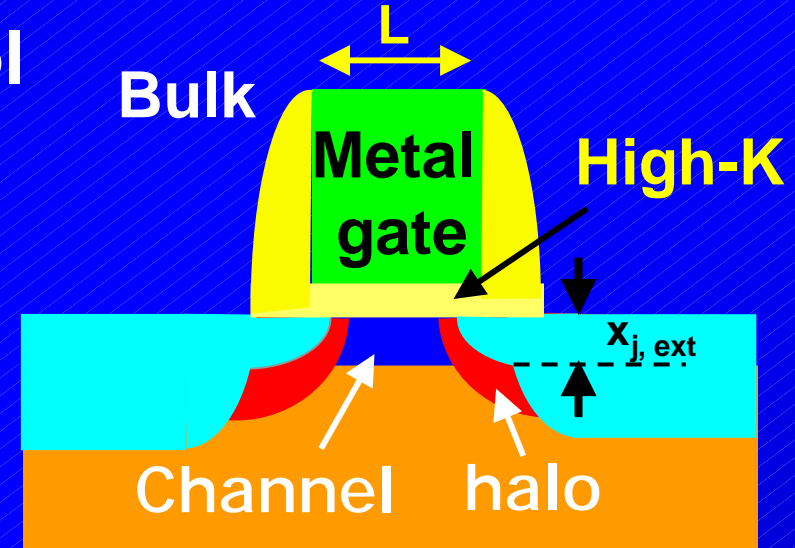
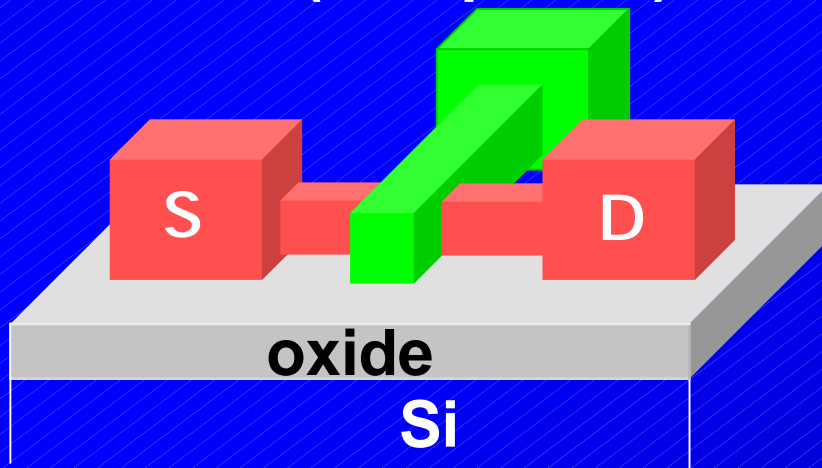


In the Future, Mobility Enhancements Will Depend on How the MOSFET Evolves (or vice-versa?)

- Must maintain good control of electrostatics
- Technology solutions:
 - Ultra-thin body (UTB)
 - Double or triple-gate structures (non-planar)

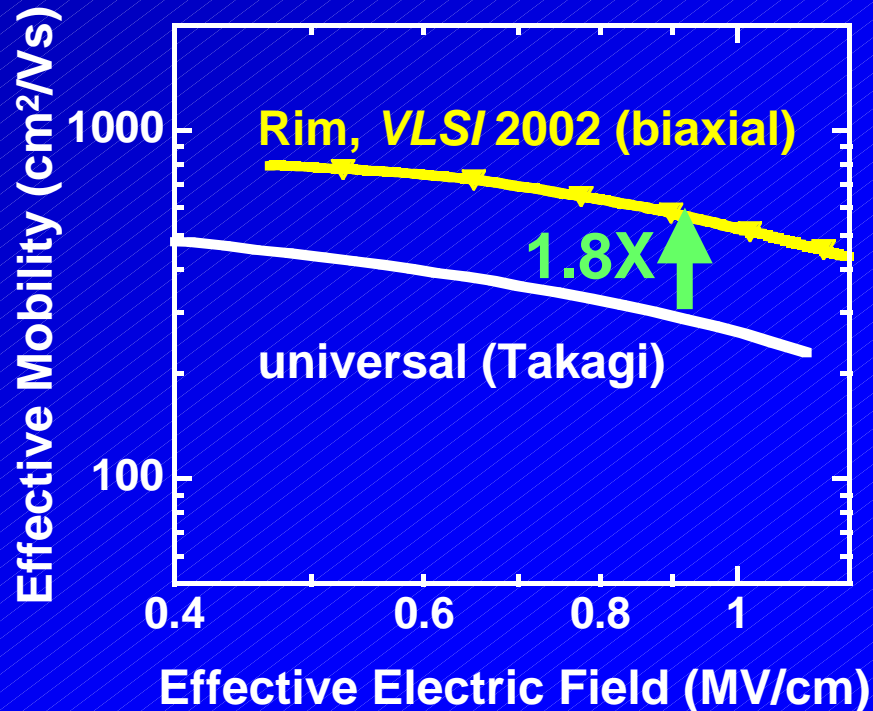


Strain Can't Do it All

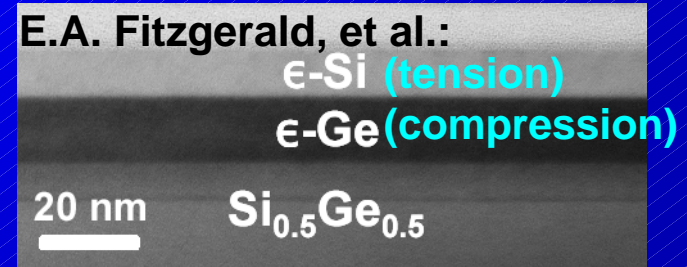
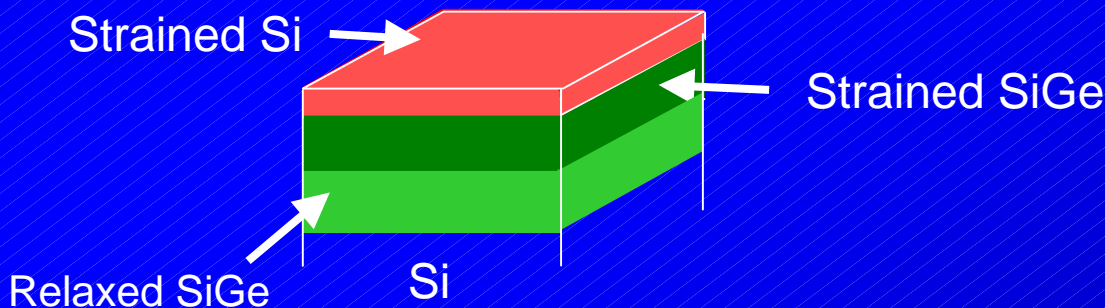
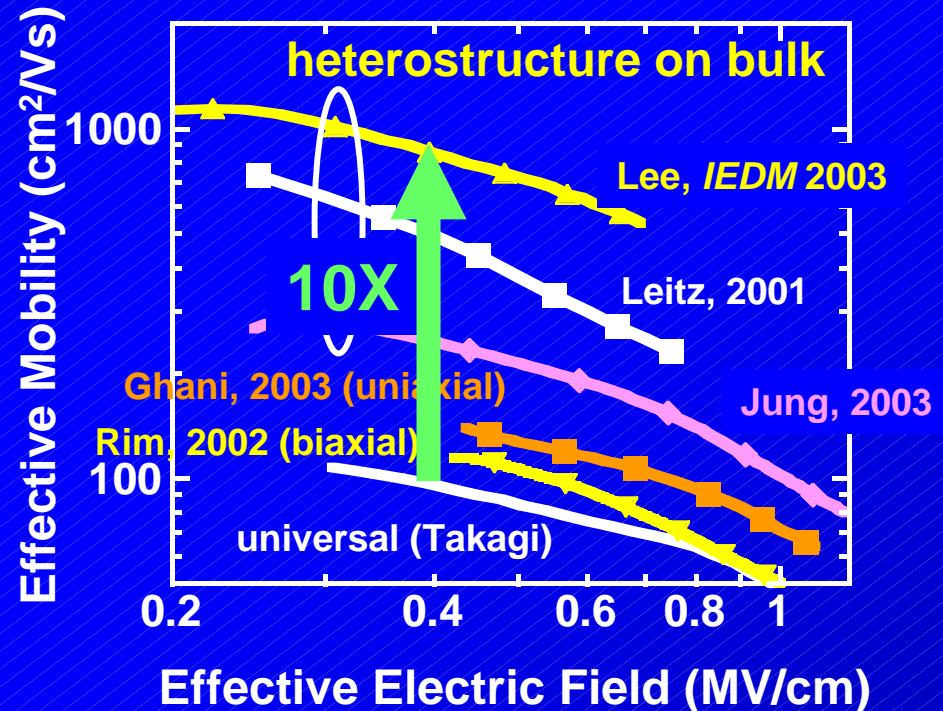
- Strain does **not** improve the Coulomb-scattering limited mobility (from ionized impurities in the channel):
 - keep channel doping below $\sim 5 \times 10^{18} \text{ cm}^{-3}$ to obtain full benefits of strain
 - UTB or non-planar CMOS promising, as channel doping can be lower than for bulk
- Need to reduce S/D series resistance in addition to channel resistance

New Channel Materials for PMOS

NMOS

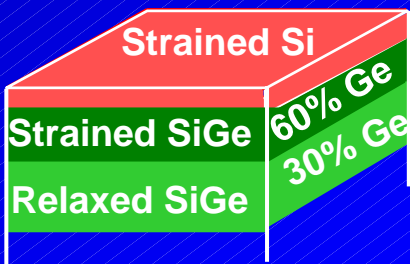
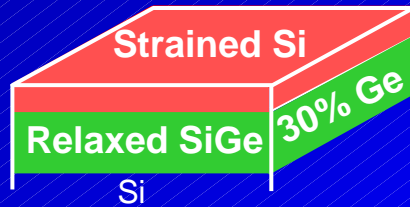


PMOS

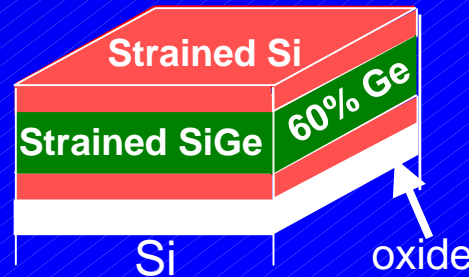


Evolution of Enhanced-Mobility Channel Materials

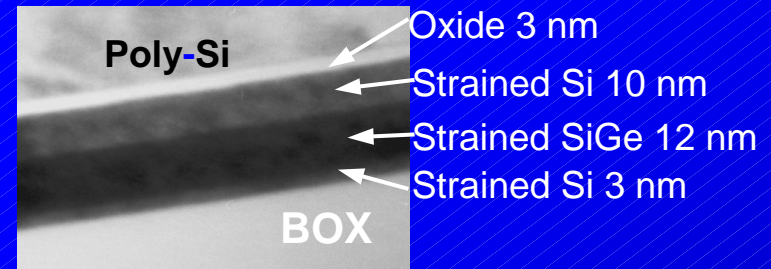
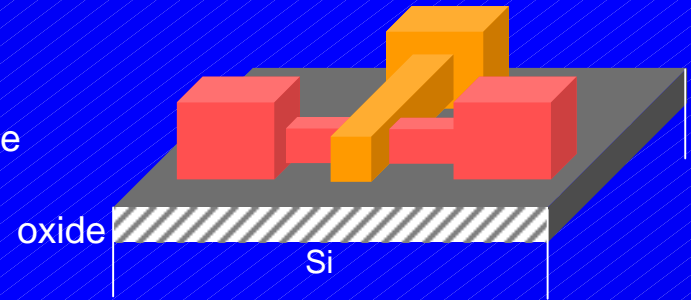
Bulk → On insulator → Non-planar?



“Heterostructure on bulk”



“Heterostructure on Insulator: HOI”

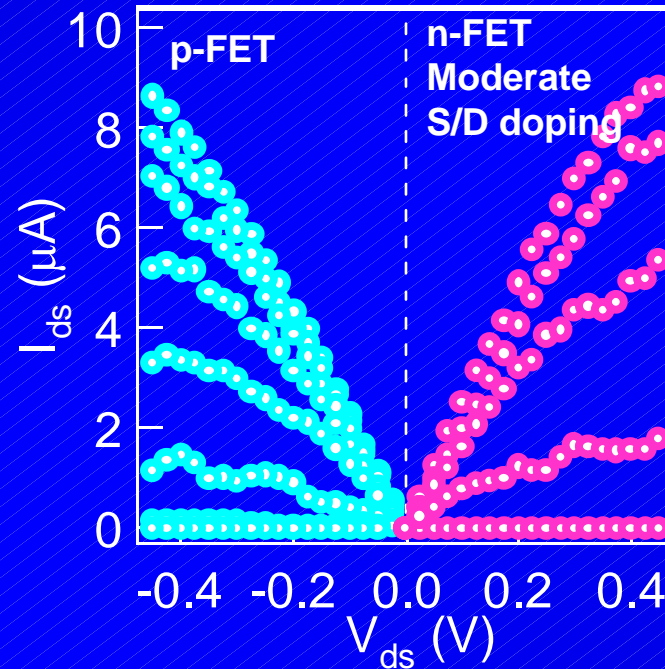
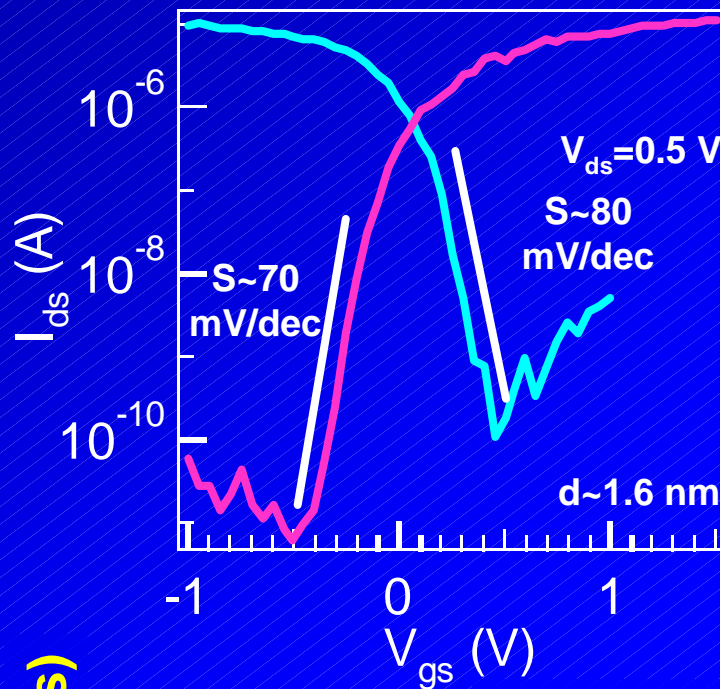


I. Aberg, et al., IEDM 2004

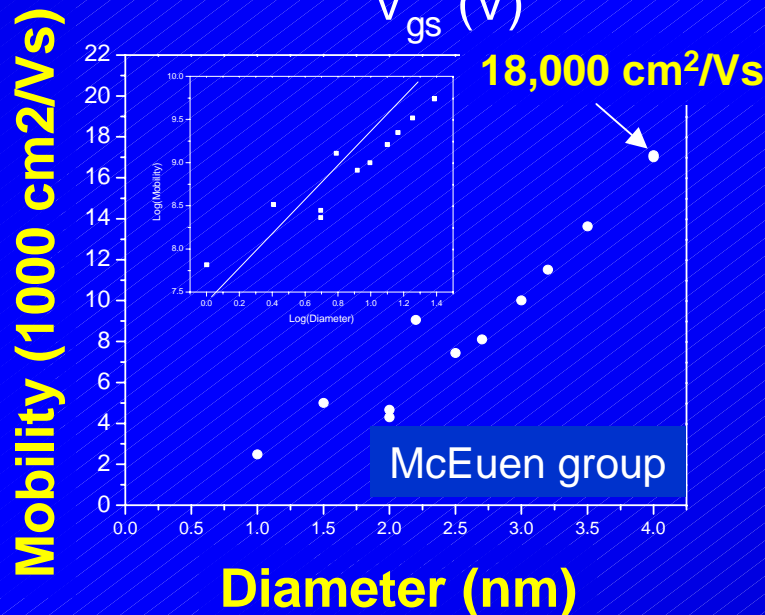
- “Hybrid” technologies and channel materials on Si platform
- Improve mobility for Ion, while also addressing electrostatics (Ioff)

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Structures and Devices

Beyond 22 nm Node: "Si CMOS plus"



Javey, A.
et al, Nano
Lett, 2005



Carbon Nanotube MOSFETs:

- Ballistic transport with good electrostatics
- Co-exist with Si CMOS

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Structures and Devices

Biggest Challenges: Takes Time and \$ To Develop New Techniques



• Don't discount possibilities too early

• Understanding of physics/materials may be "wrong": e.g.

"Everyone knows mobility won't be important for sub-100 nm"

New Device Structures for 32 nm Node and Beyond

- Bulk or planar SOI, and when?
 - 32 and 22 nm nodes will probably be bulk for HP, or thin-body SOI for some applications
- FinFET or tri-gate, and when?
 - Tri-gate may be more manufacturable, so perhaps will be first, and progress to more FinFET-like geometry
 - Seems that introduction will be at 22 nm or beyond
- Global strain, local strain, or other techniques, and when?
 - Combinations of global and local stress may be needed
 - Hybrid orientation (100) NMOS and (110) PMOS is interesting
 - Will need alternate channel materials (SiGe or Ge p-MOS, GaAs n-MOS)
- For high-performance or low-power applications?
 - High-performance will likely drive non-planar, with LSTP next
- Si nanowire or C nanotube FET?
 - Perhaps ultimate combination of transport and electrostatics
 - Co-exist with Si CMOS, beyond 22 nm node