

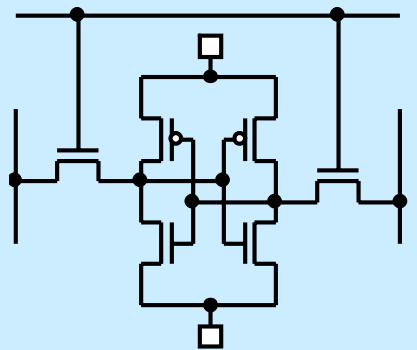
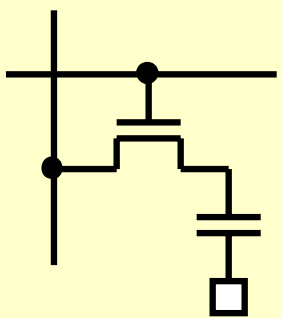
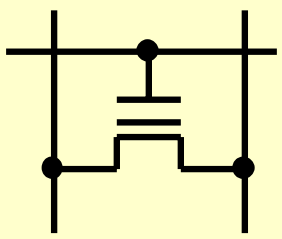
***IFST 2005***  
***19-21 June 2005, Yokohama, Japan***

***Overview of Future Memory Devices***  
***- from Stacked Memory, Gain Memory,***  
***SEM to Molecular Memory***

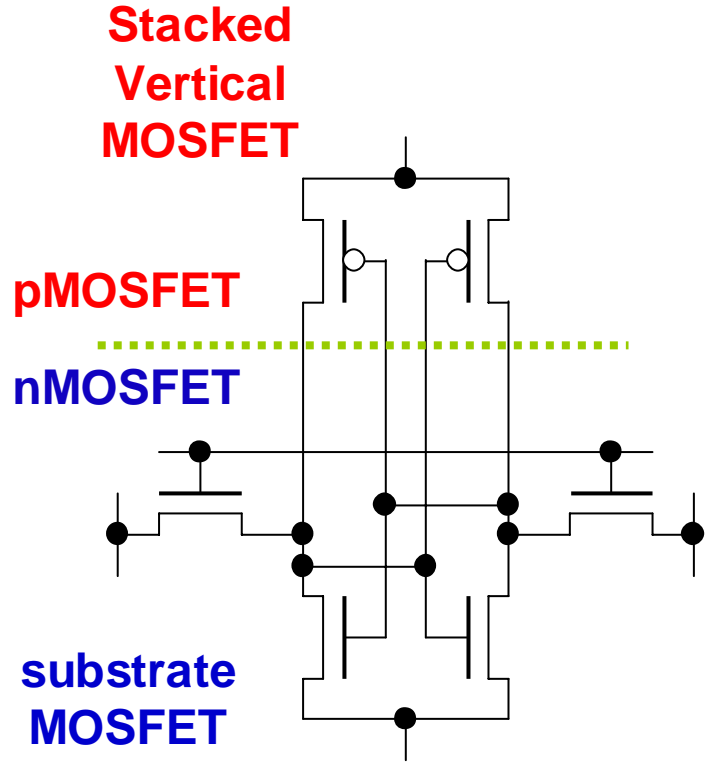
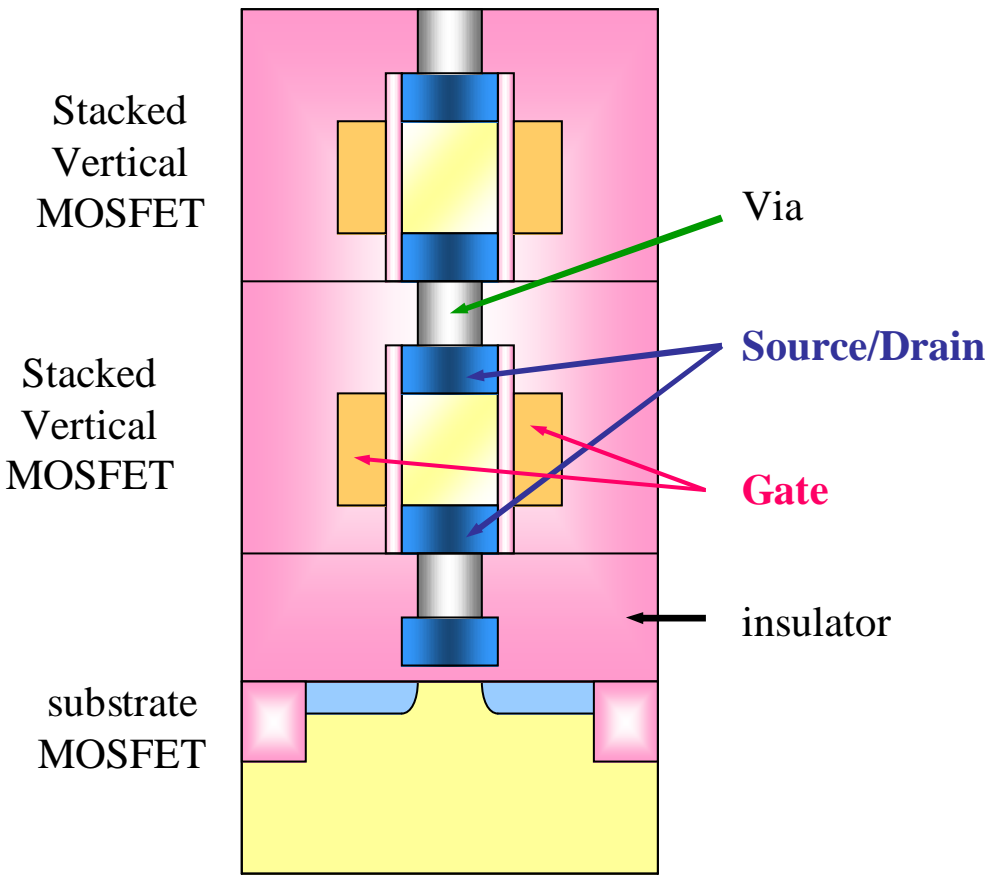
Kazuo Nakazato

Nagoya University

# Semiconductor Memories

Memory	SRAM	DRAM	FLASH
Feature	high-speed low power	low cost high-density high-speed	low cost high-density ROM
Application	server, CPU cache memory	computer main memory	mobile equipment replacement of hard disk
Memory Cell			
Cell Size	130 F <sup>2</sup>	6 - 8 F <sup>2</sup>	4 - 10 F <sup>2</sup>
Access Time	10 ns	40 ns	10 μs

# Stacked Vertical MOSFET



no PWELL-NWELL isolation

# Why Stacked Vertical ?

## 3-d Memory Cell

**stacked**  $\Rightarrow$  polycrystalline silicon channel



performance degradation when carriers transport across grain boundaries

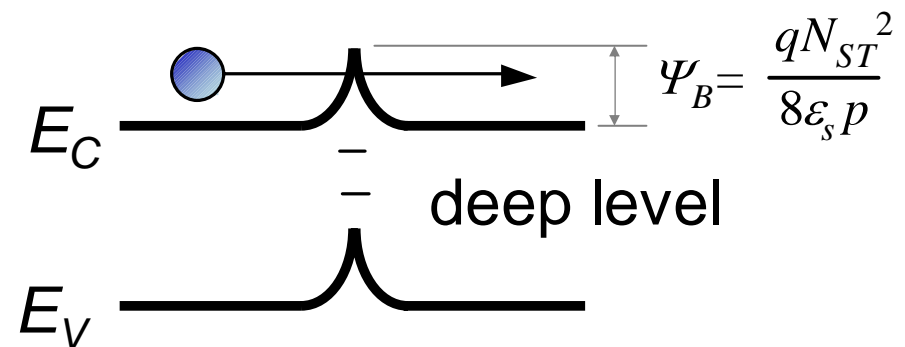
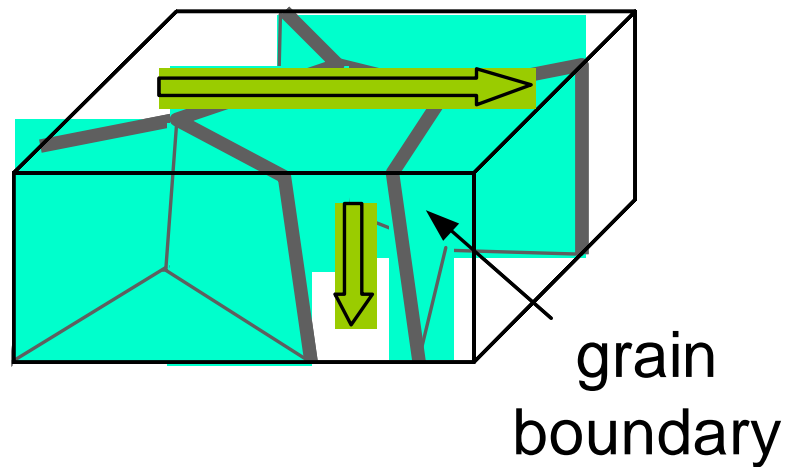


columnar or disc-shaped grains



**vertical**

carrier flow mainly without crossing any grain boundaries



$\Psi_B$  : barrier height of grain boundary

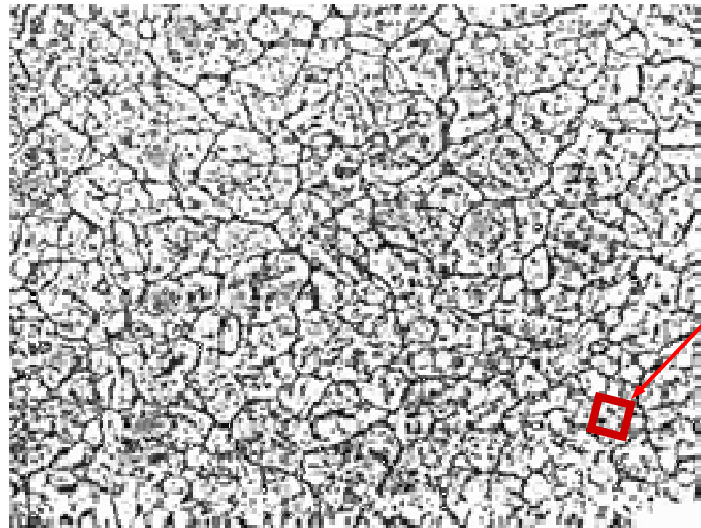
$N_{ST}$  : trap density at grain boundary

$\epsilon_s$  : silicon permittivity

$p$  : carrier density

# Example of Distribution of Grain-boundaries

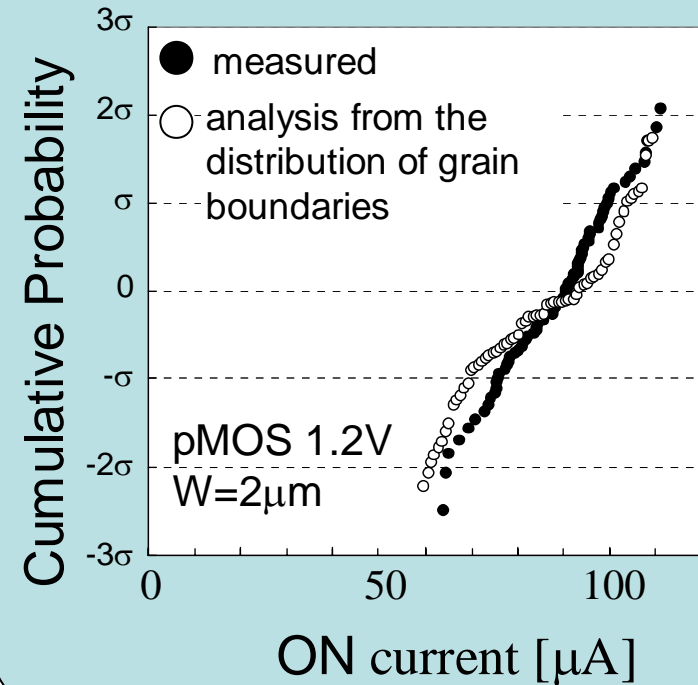
Distribution of ON currents of SV-MOSFET



transistor size  
(0.2 $\mu\text{m}$  x 0.2 $\mu\text{m}$ )

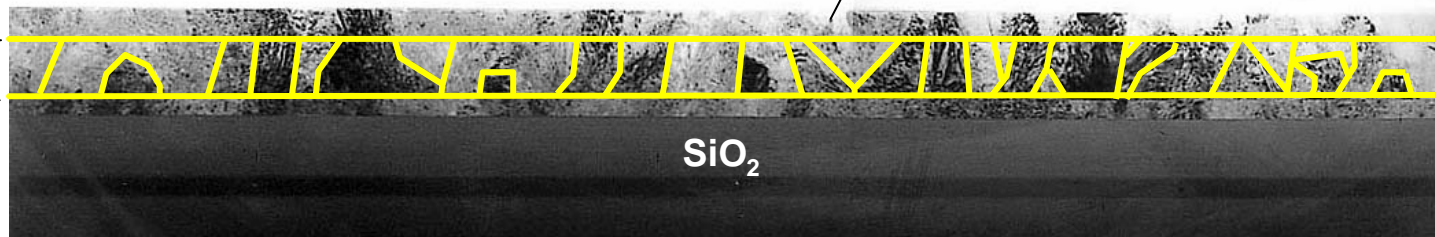
plan view

3 $\mu\text{m}$



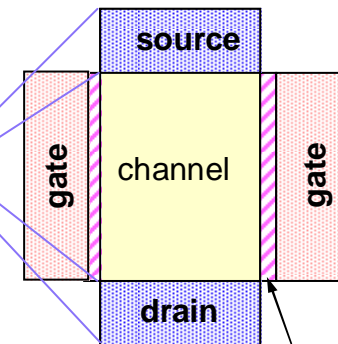
300nm

cross sectional view



polycrystalline silicon

SiO<sub>2</sub>

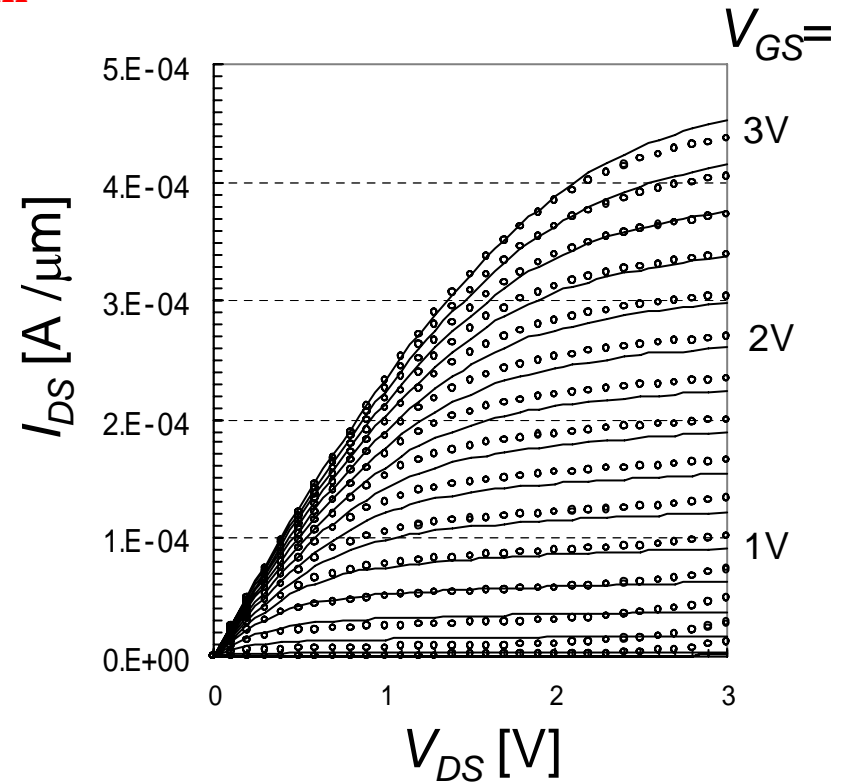
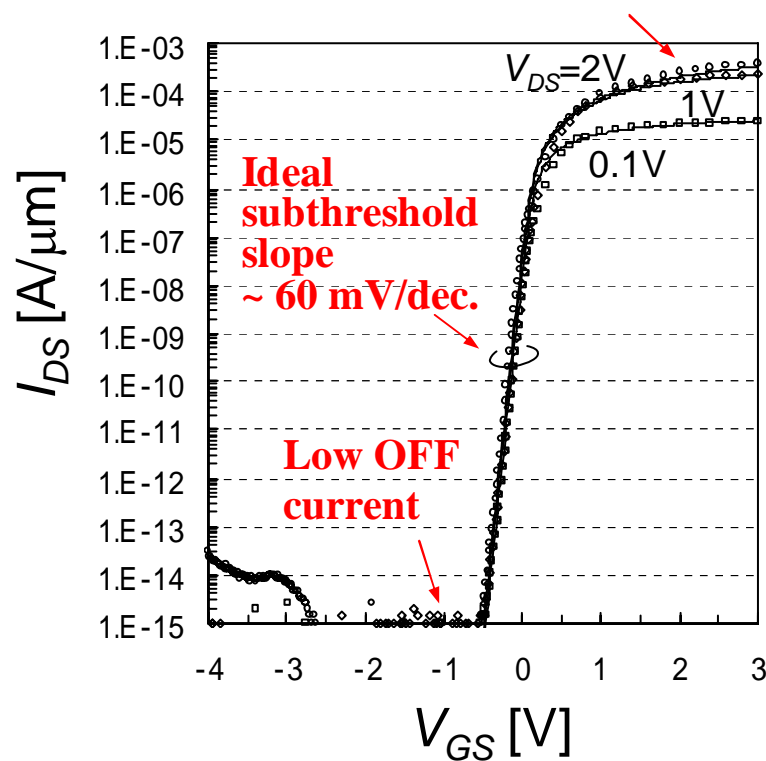


gate oxide

# Characteristics of SV-MOSFET

*show very similar to single-crystal MOSFET*

**High ON current  $\sim 300\mu\text{A}/\mu\text{m}$**



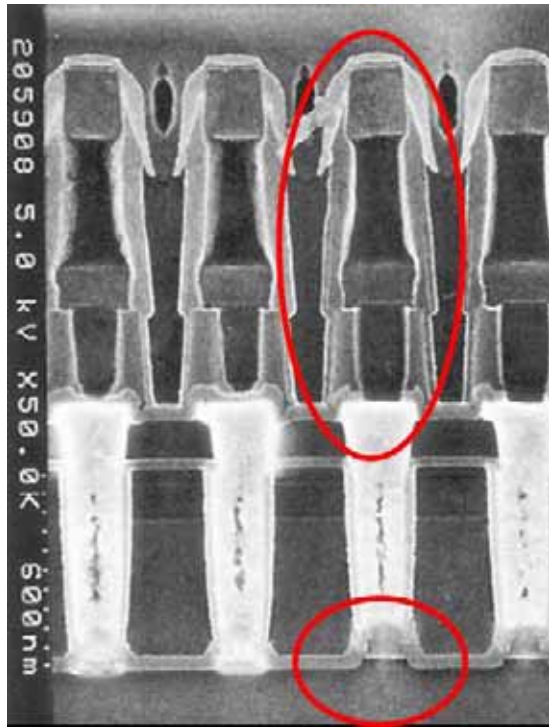
○ measured  
— device simulation with  $300\text{ cm}^2/\text{Vs}$

**NMOS**

# Characteristics of *p*-type SV-MOSFET stacked on substrate MOSFET

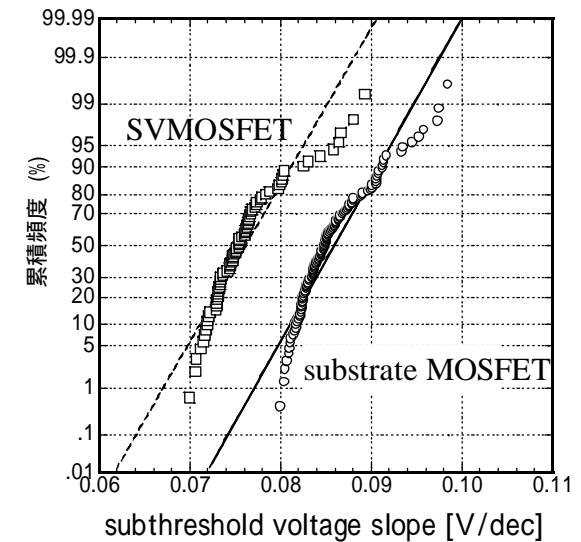
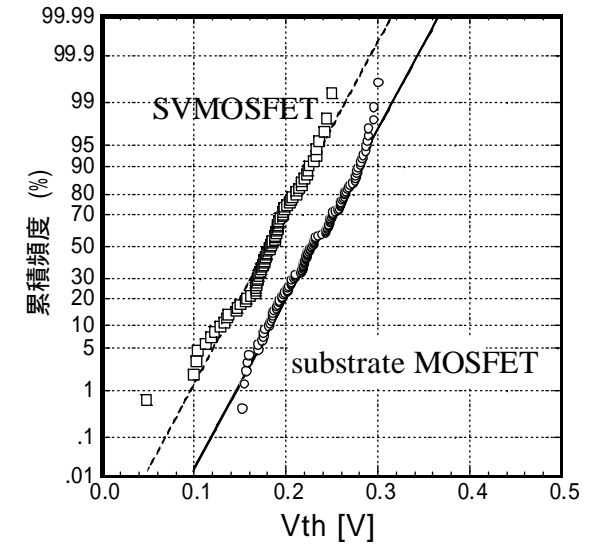
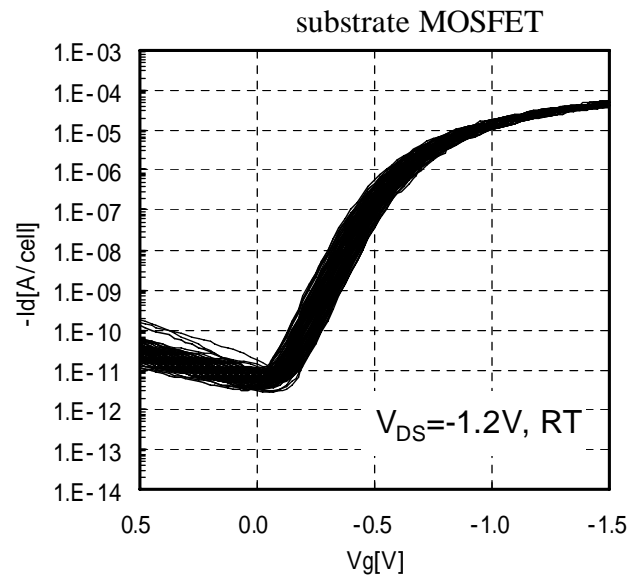
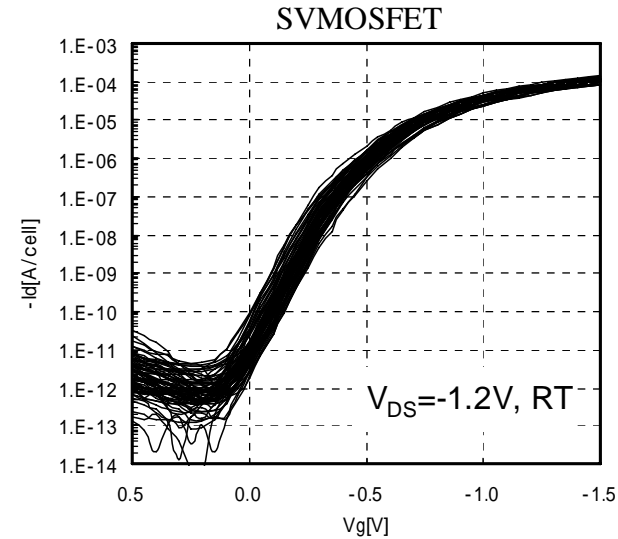
**PMOS**

SV-MOSFET



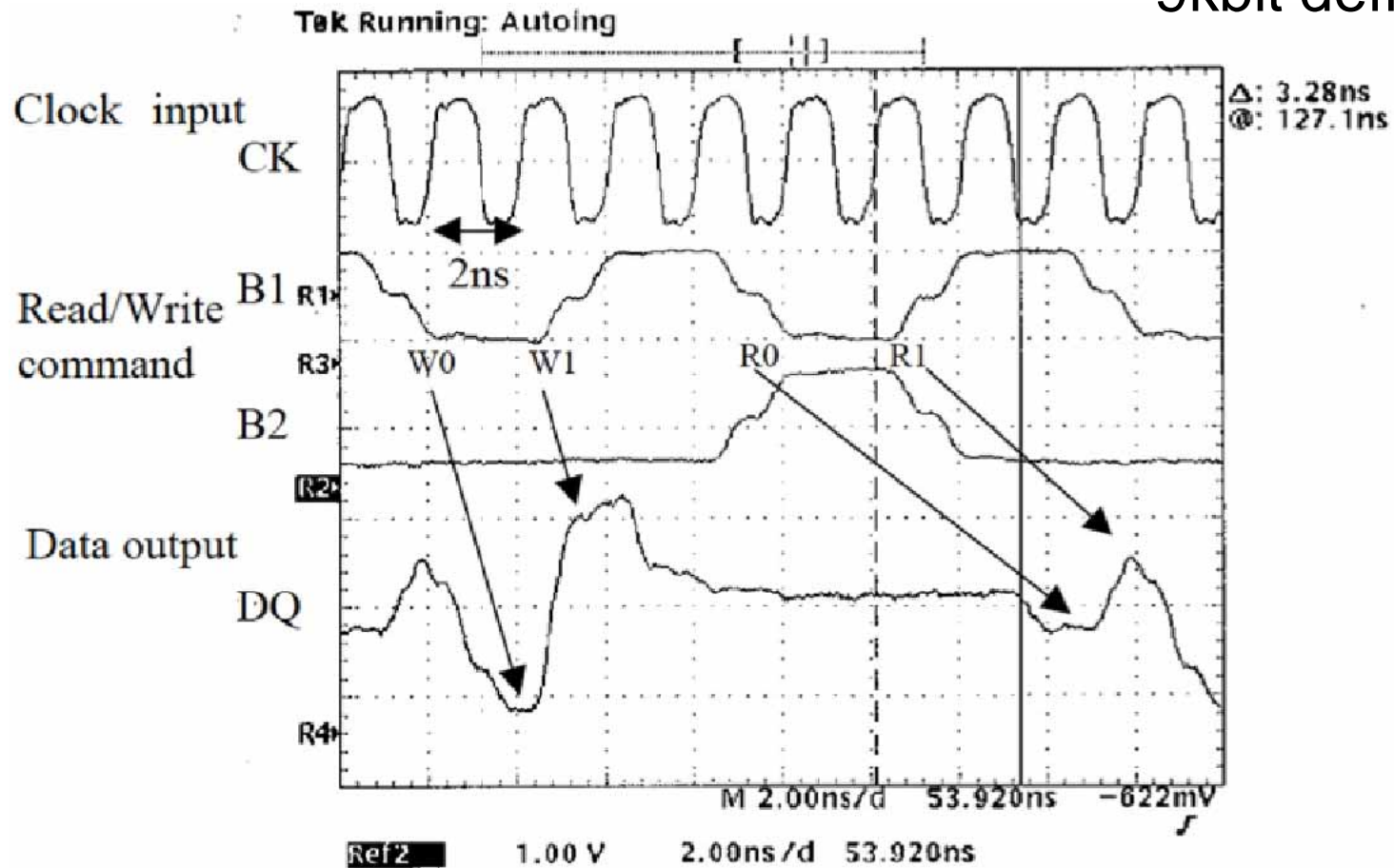
substrate MOSFET

H Matsuoka, T Mine, K Nakazato, M Moniwa, Y Takahashi, M Matsuoka, H Chakihara, A Fujimoto, and K Okuyama, Symp. VLSI Technol. Dig. Papers 2004



# 533MHz 64Mbit SRAM

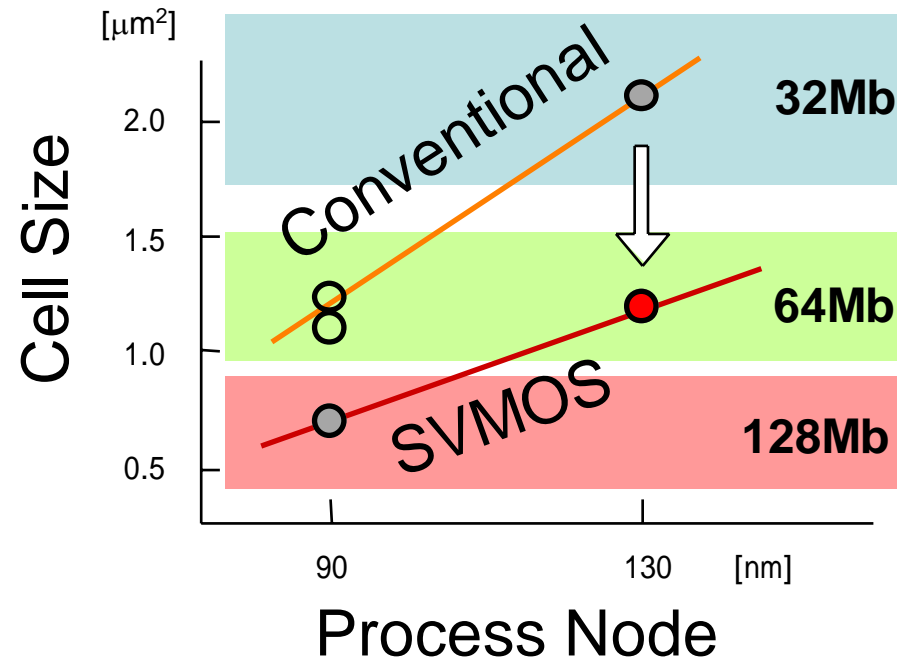
9kbit deficit



T Kikuchi, S Moriya, H Matsuoka, K Nakazato, A Nishida, H Chakihara, M Matsuoka, and M Moniwa, IEDM Dec. 2004



# SRAM Cell Size vs Process Node

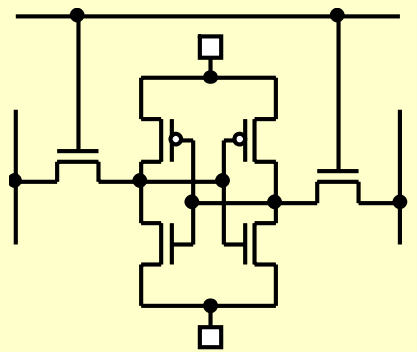
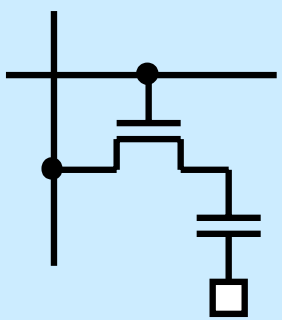
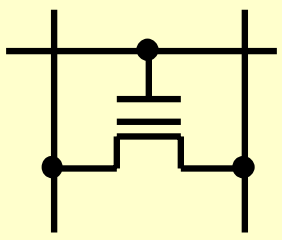


Cell size of next generation can be achieved by the present process node

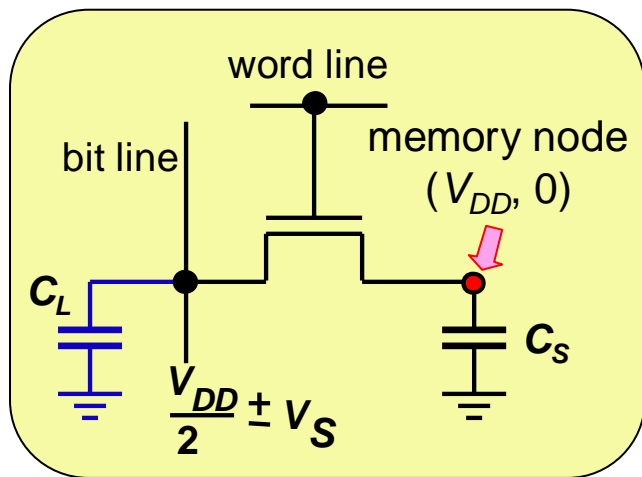
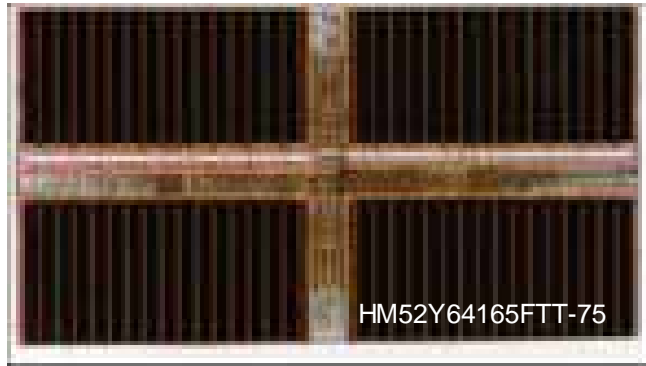


Huge investment is required for setting up next process node.  
Memory with minimum cell size may become standard cell finally.

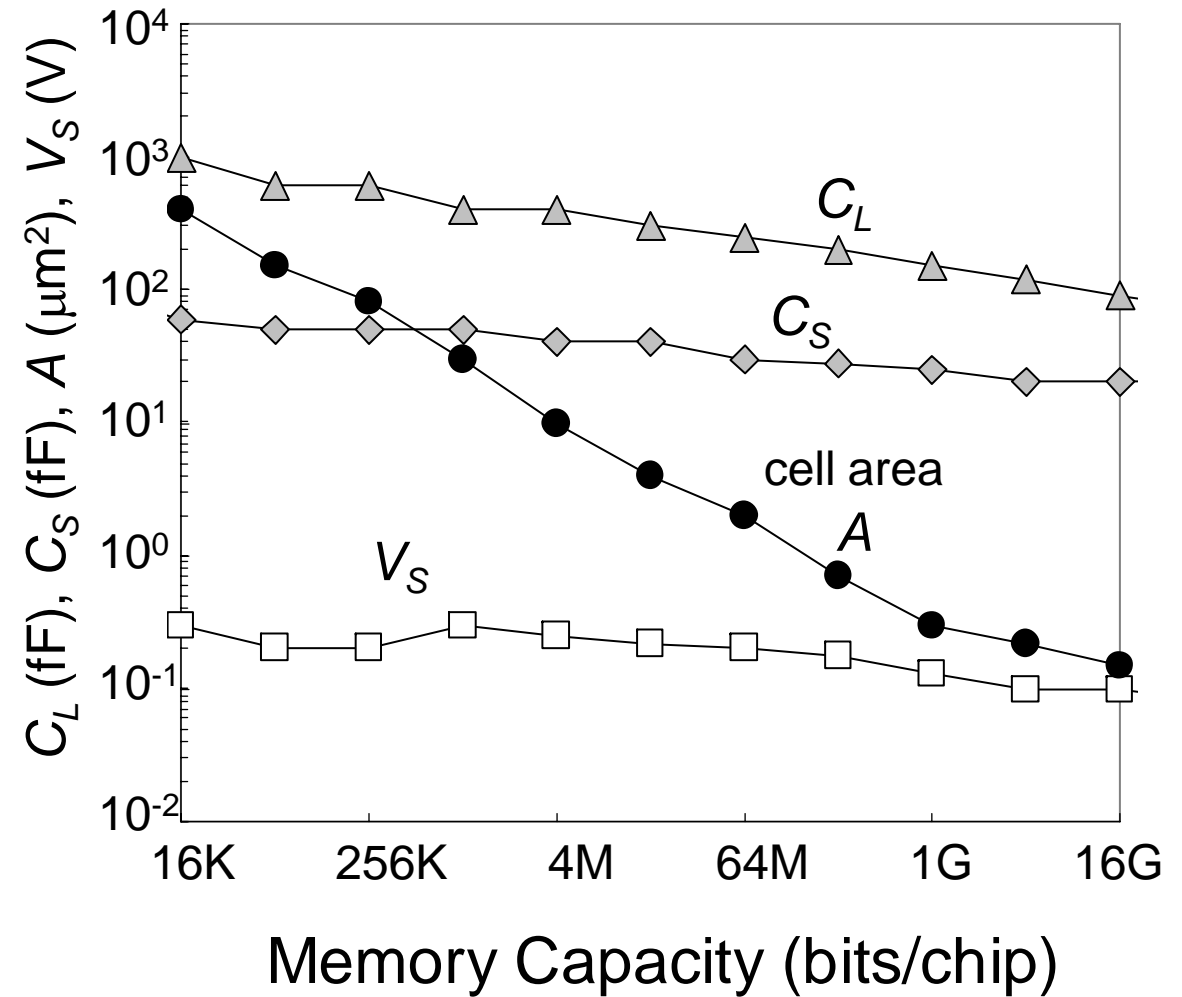
# *Semiconductor Memories*

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Memory Cell			
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Access Time	10 ns	40 ns	10 μs

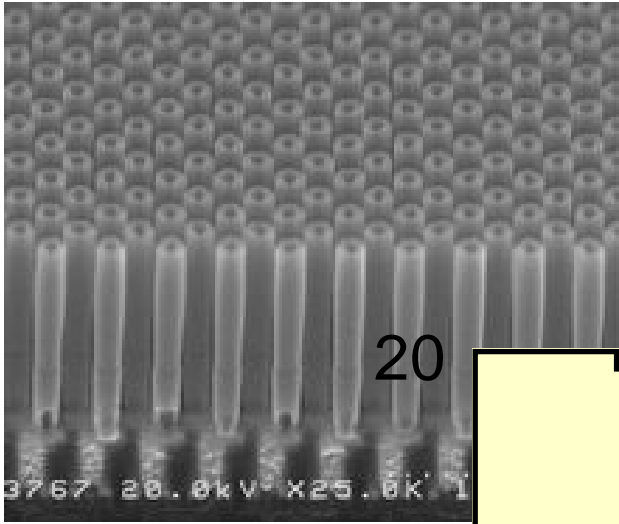
# DRAM 1-T cell



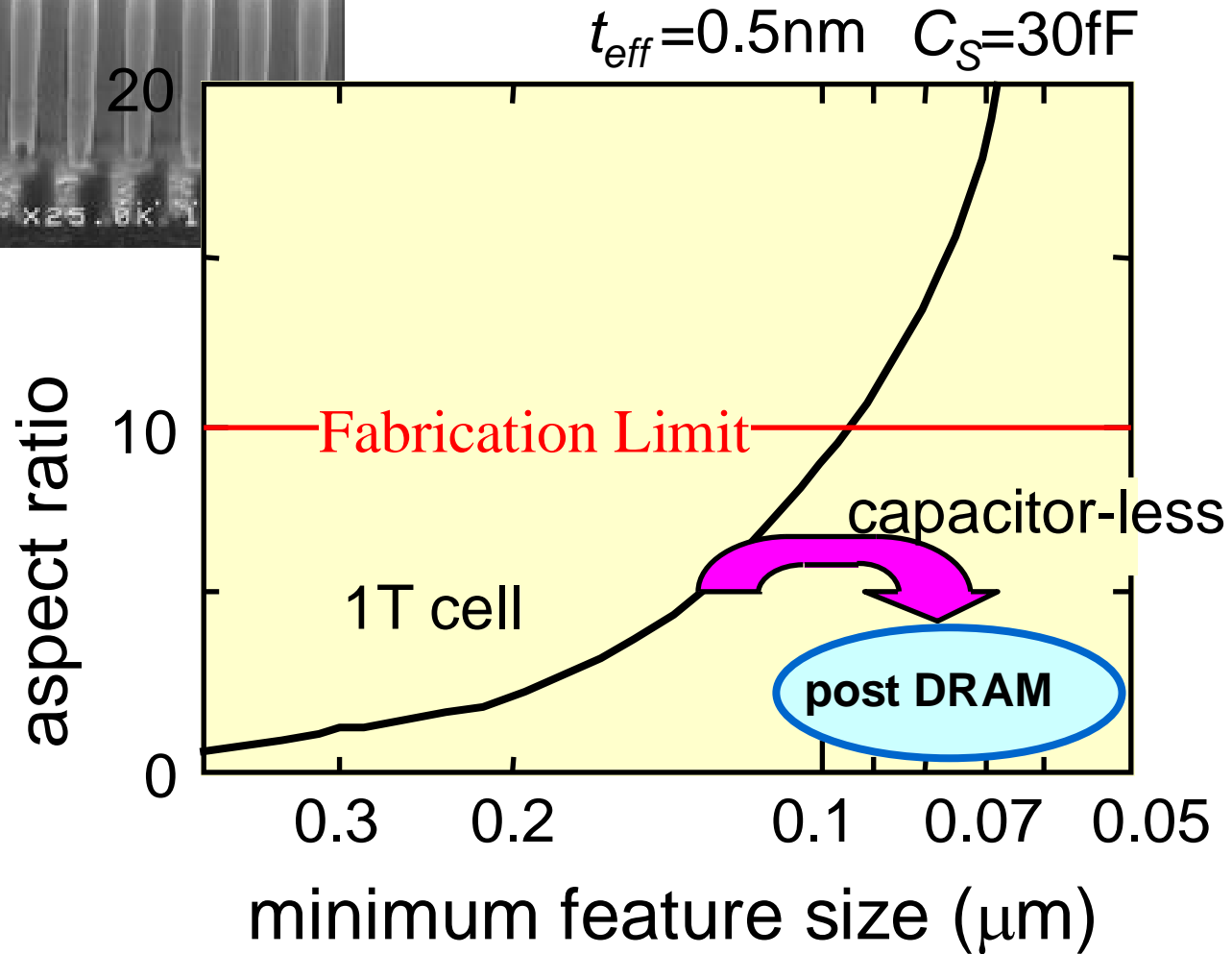
$$V_S \sim \frac{V_{DD} C_S}{2C_L}$$



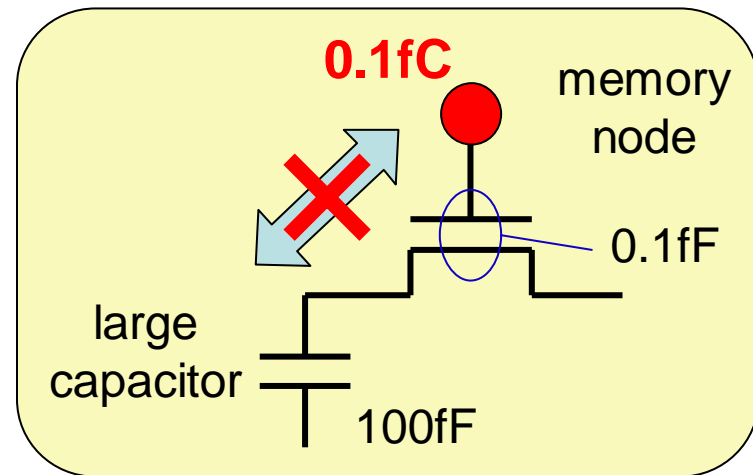
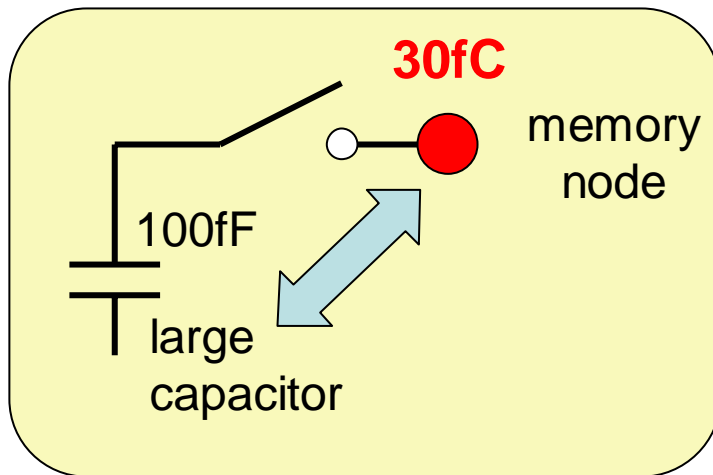
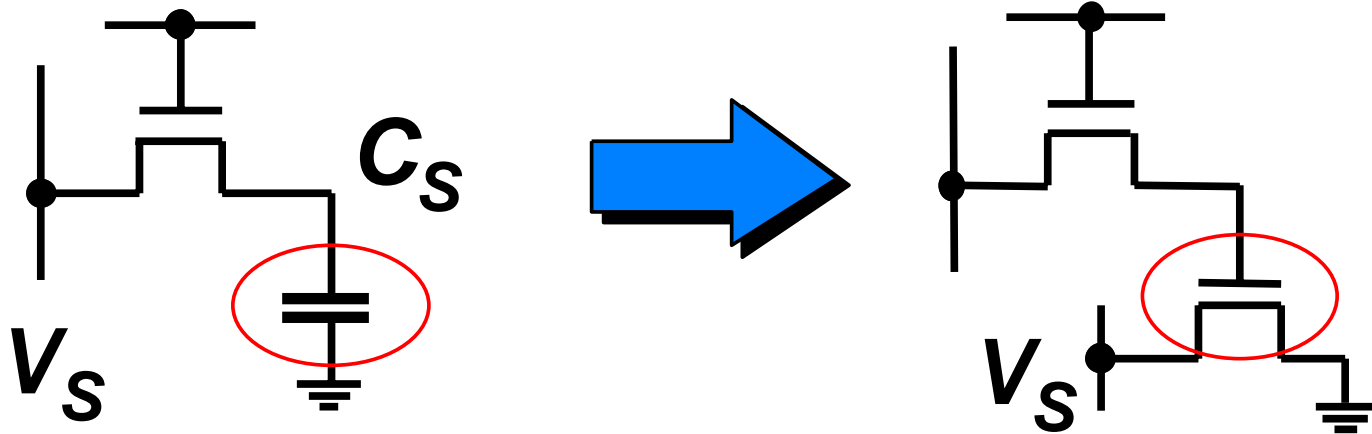
# post DRAM cell



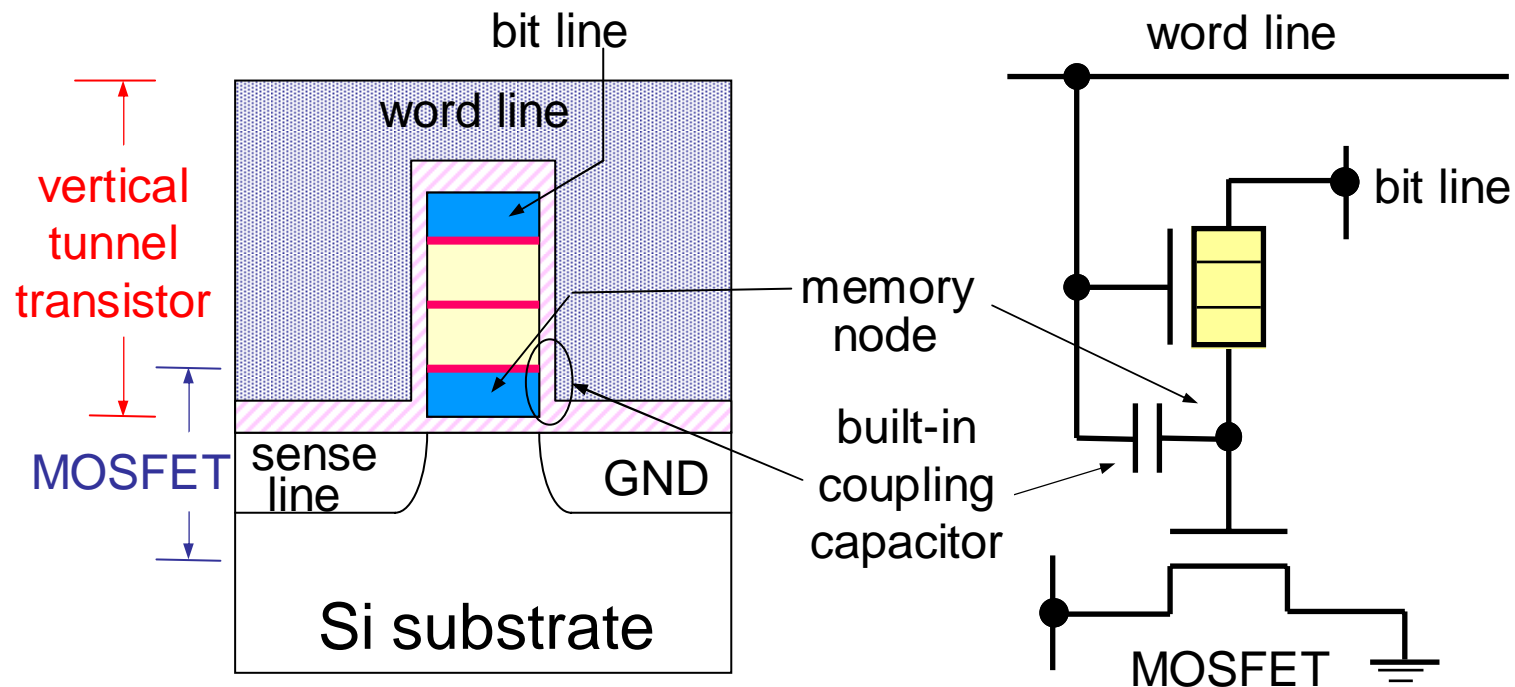
J.M.Park et al  
IEDM 2002



# Gain Cell



# PLEDM - memory cell



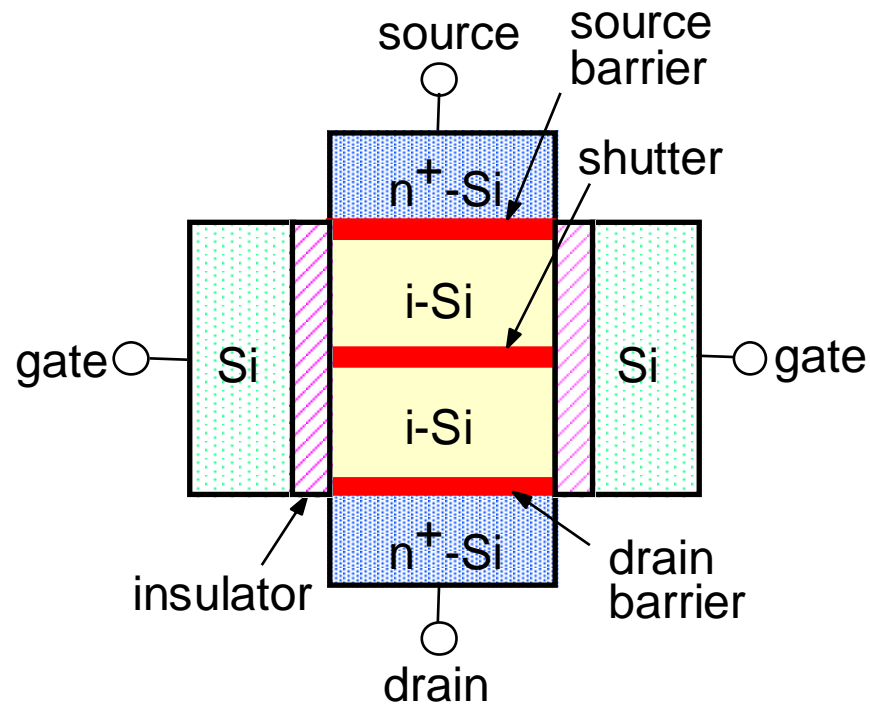
Stacked structure

- Minimum sized gain cell (~ half of DRAM 1-T cell)

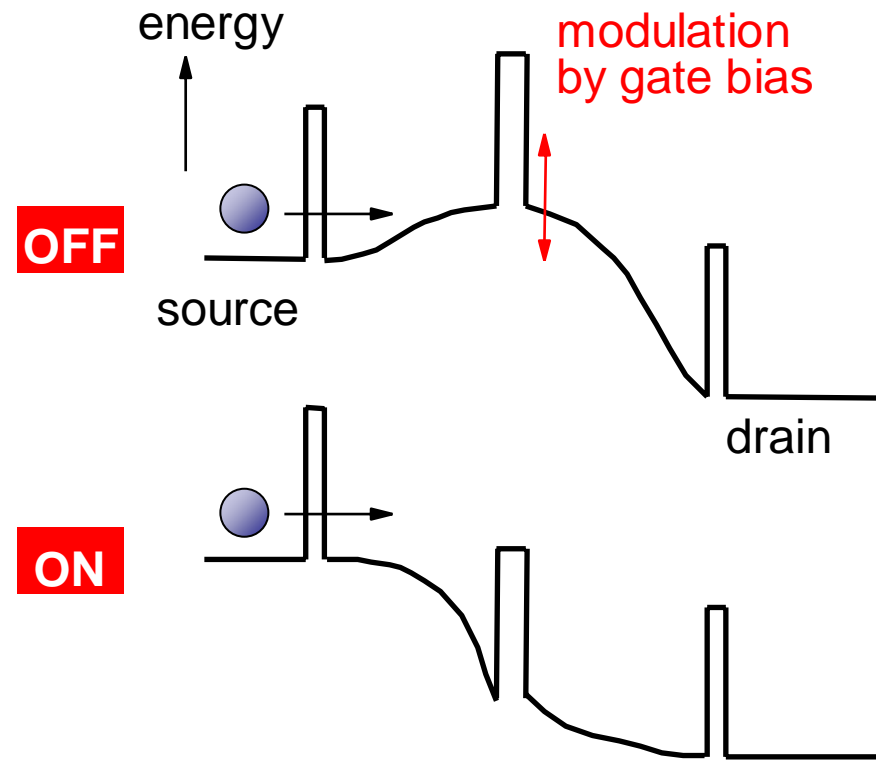
Tunnel transistor

- high ON/OFF current ratio (high speed/long retention time)

# Stacked Tunnel Transistor - PLEDTR

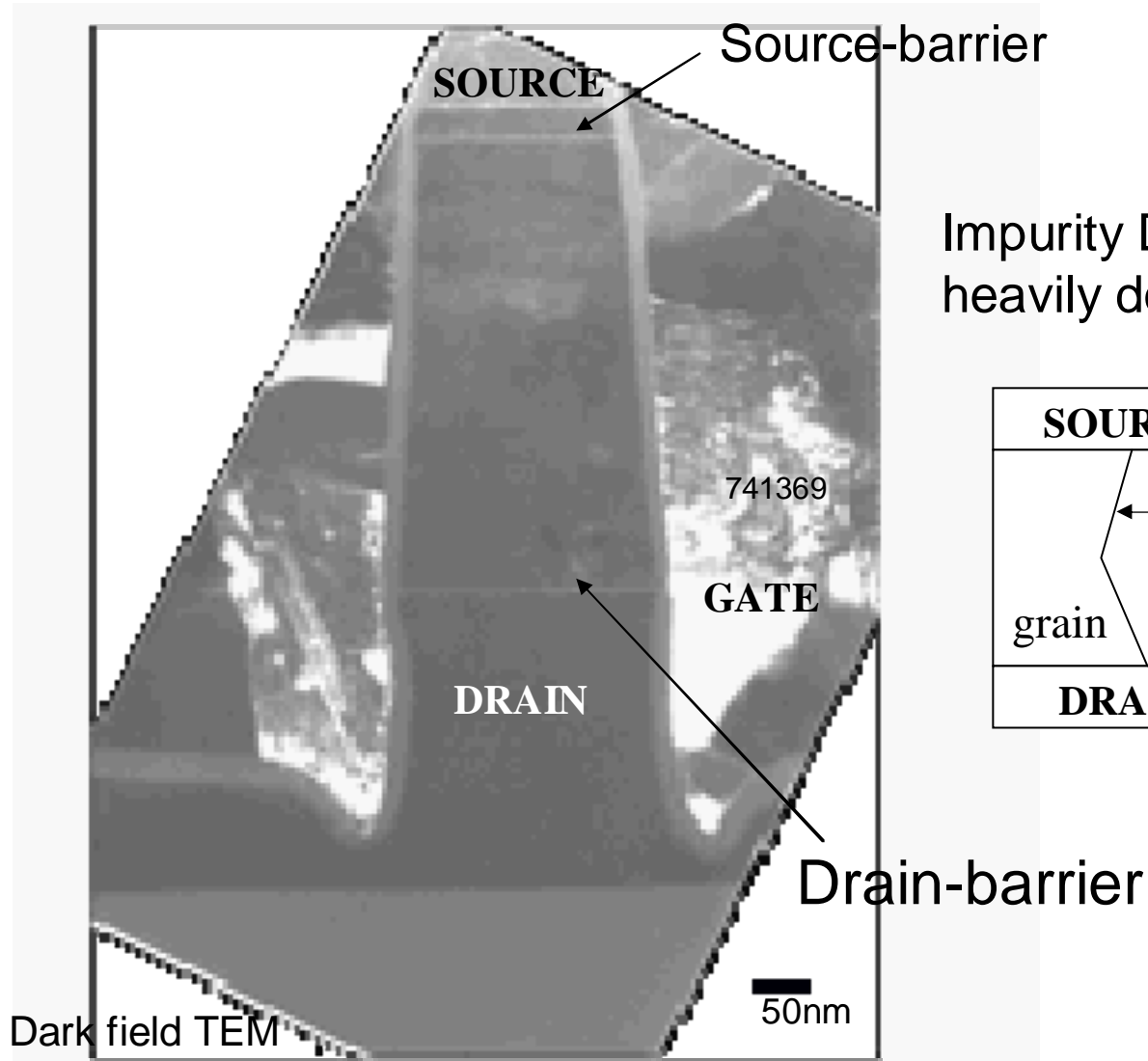


(a) Schematic cross-sectional view showing device operating principle

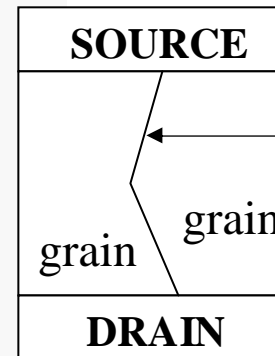


(b) Conduction band energy diagram

# Source/Drain Barriers



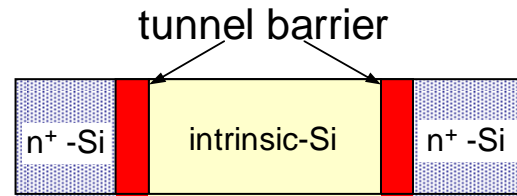
Impurity Diffusion Barrier from heavily doped source/drain



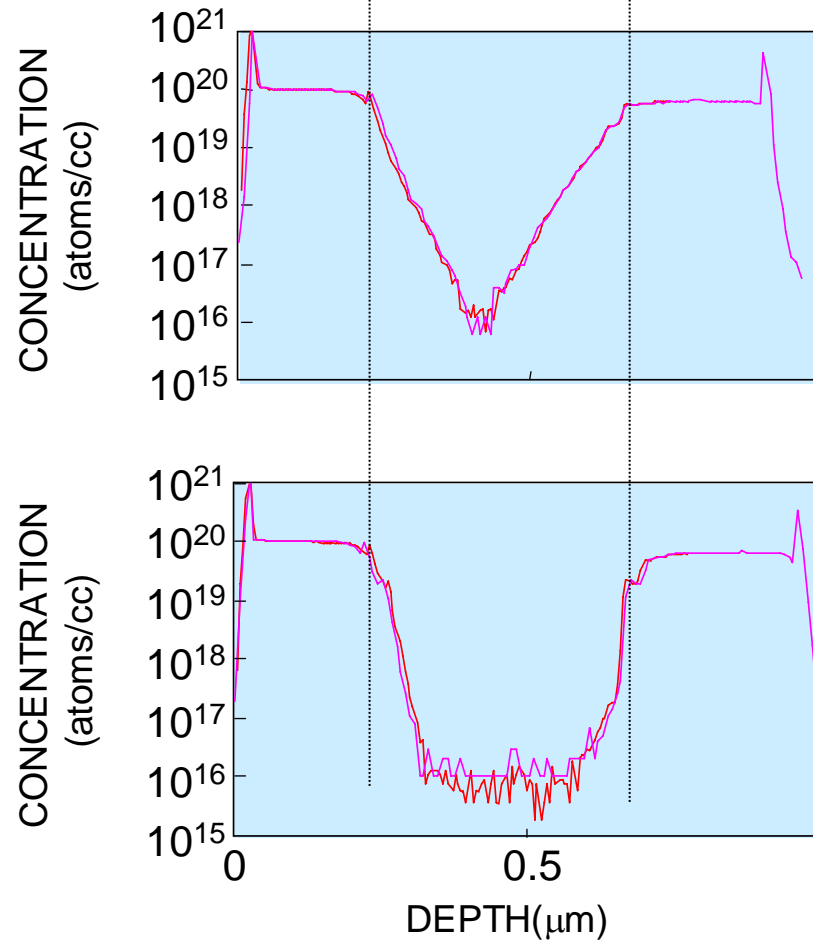
*Diffusion constant through grain boundaries is more than 100 times higher than the diffusion constant in grain.*



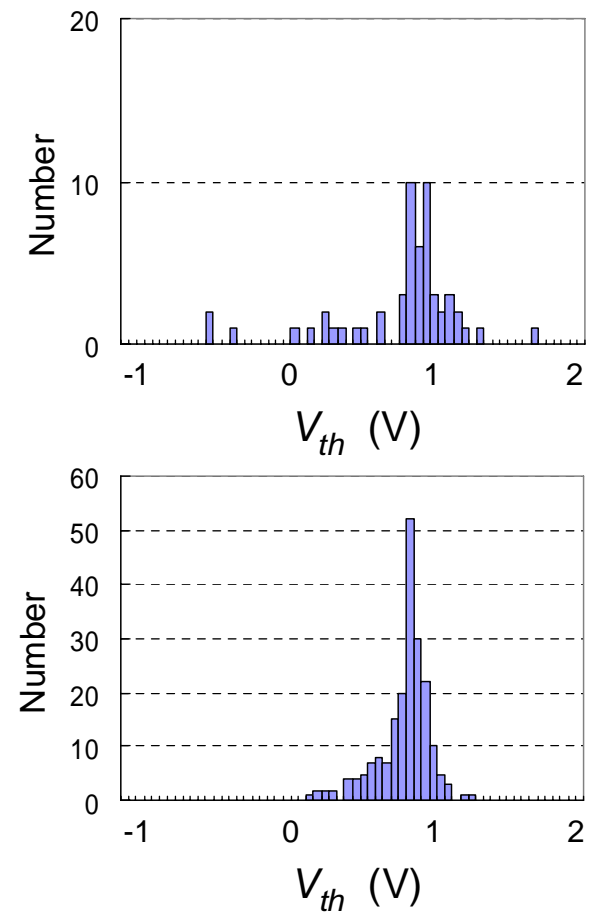
# Effect of Source and Drain Barriers



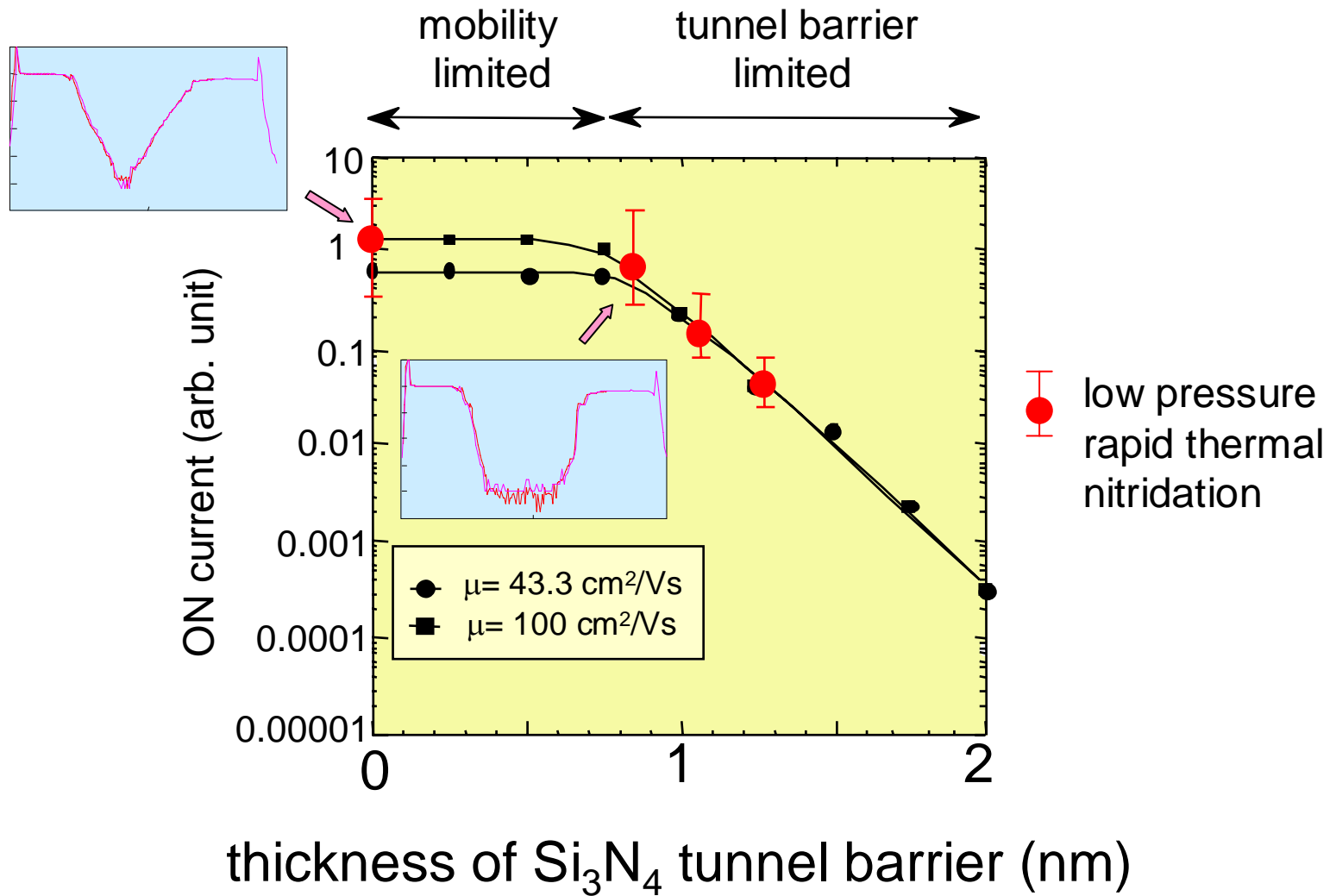
without tunnel barrier



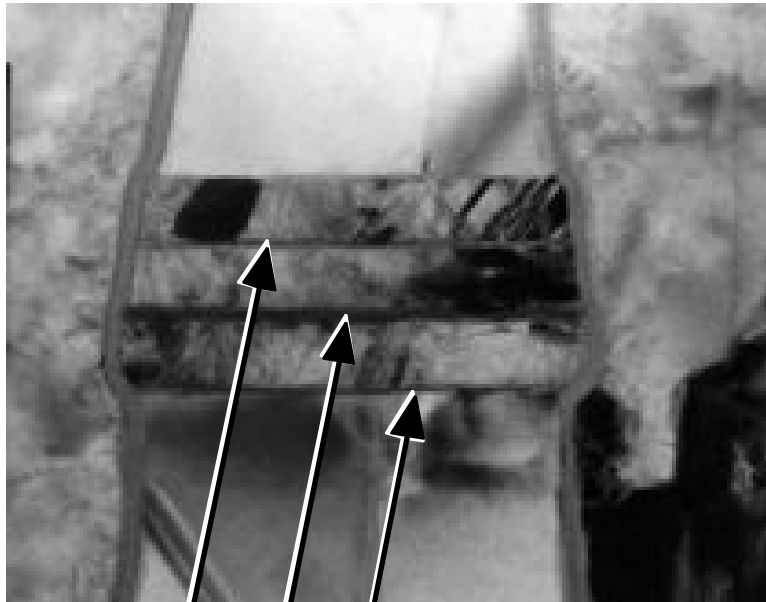
distribution of threshold voltage



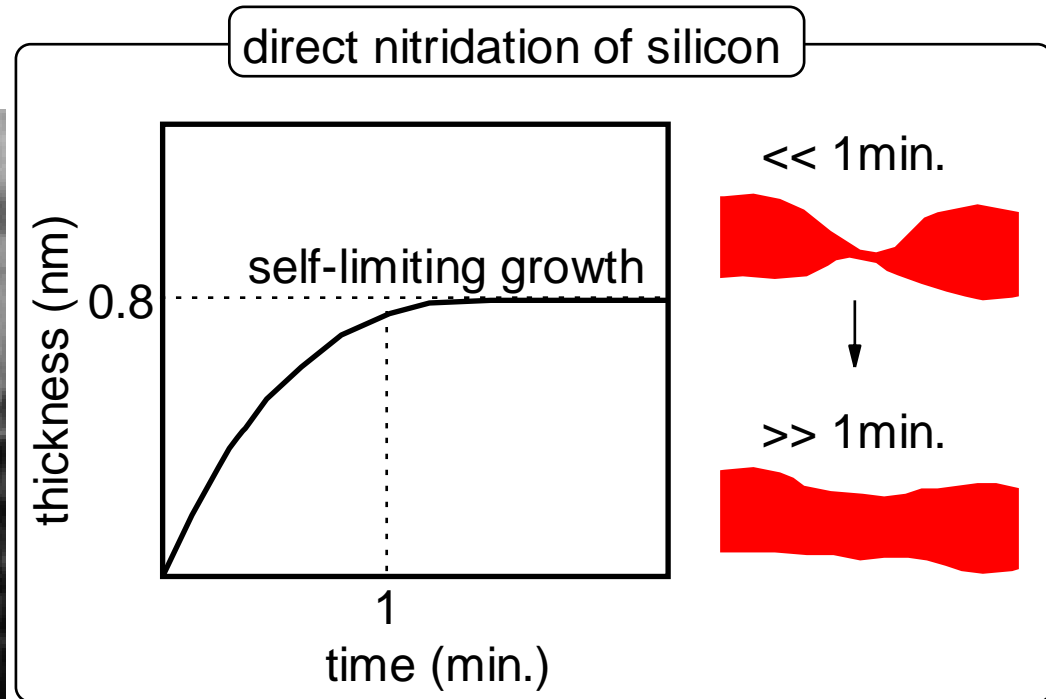
# ON current



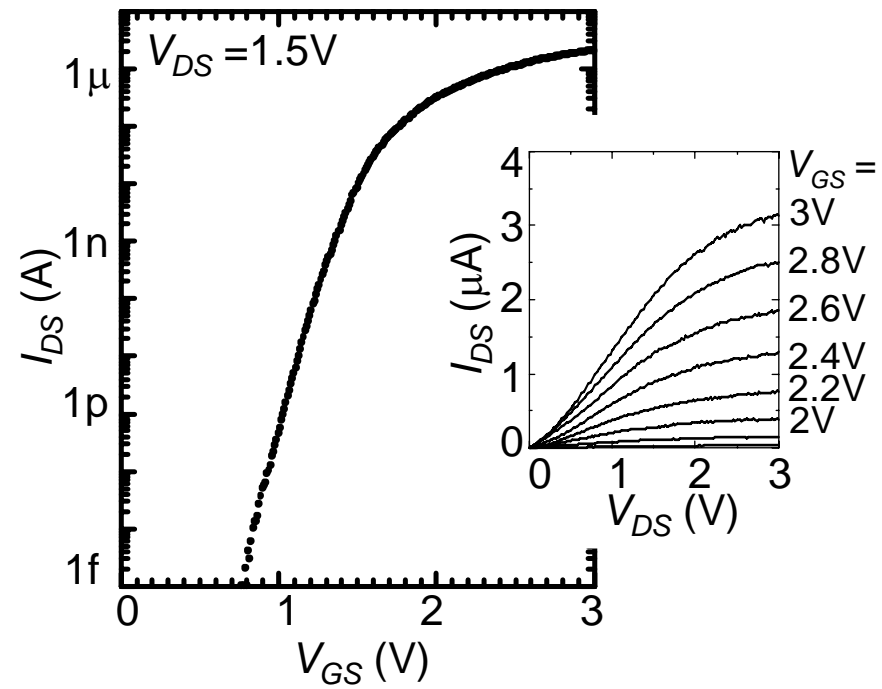
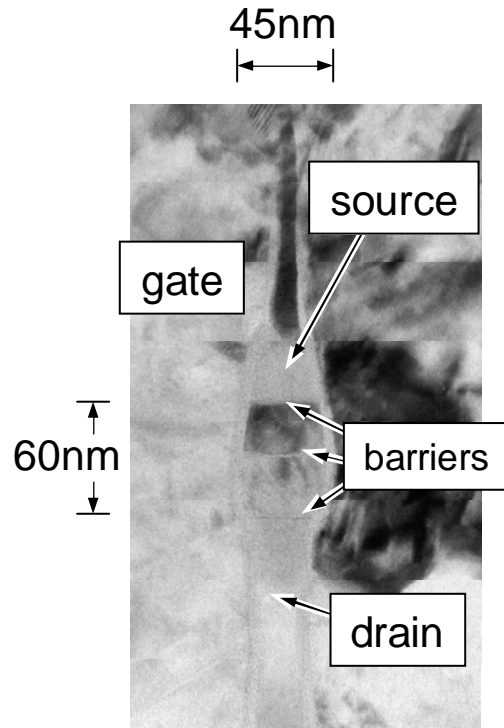
# Formation of Stable Thin Tunnel Barriers



drain barrier  
shutter barrier  
source barrier

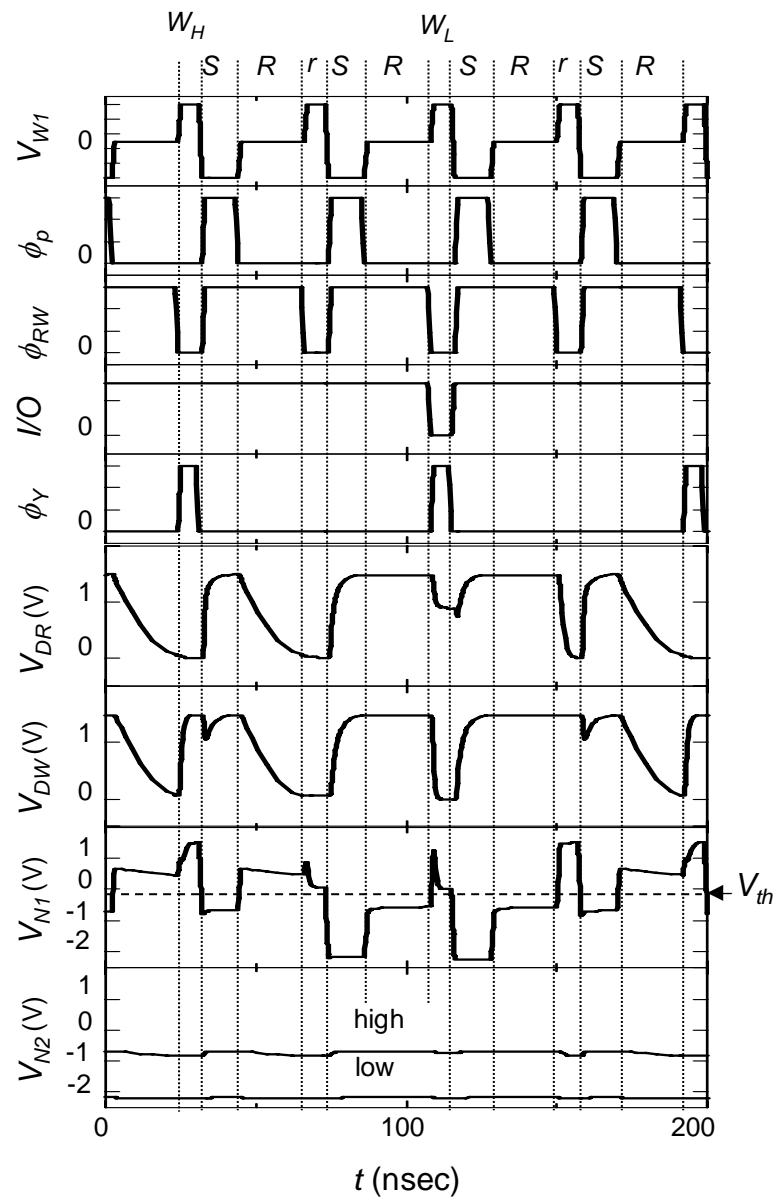
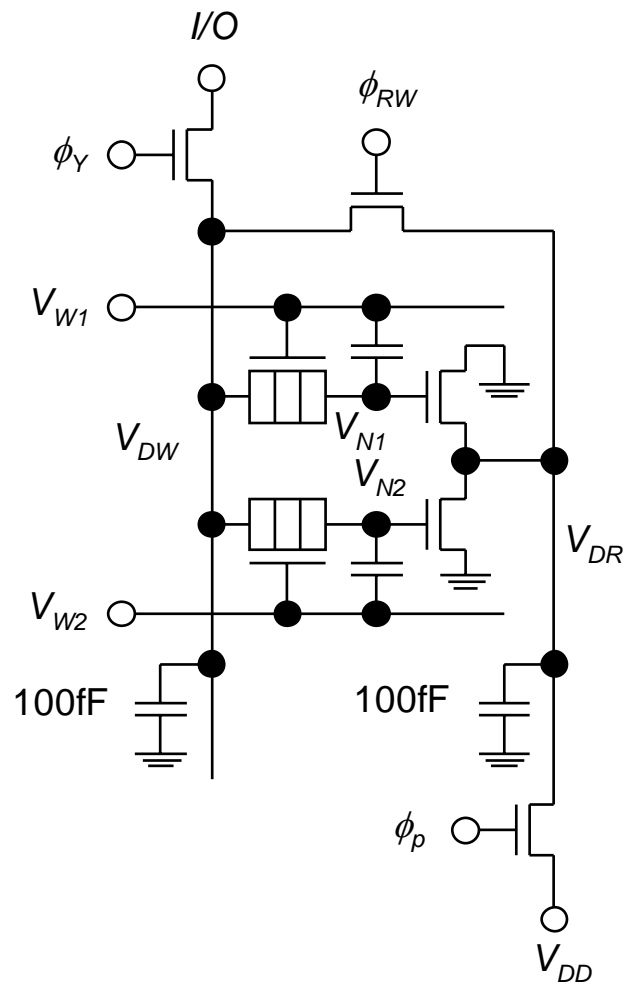
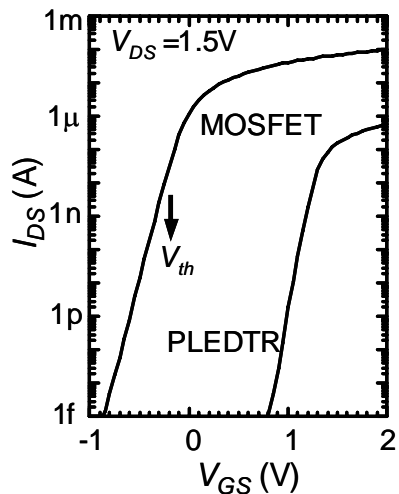


# 60 nm channel PLEDTR



K Nakazato, K Ito, H Mizuta, and H Ahmed  
Electron. Lett., 35 (1999), pp.848-850

# Operation of PLEDM device

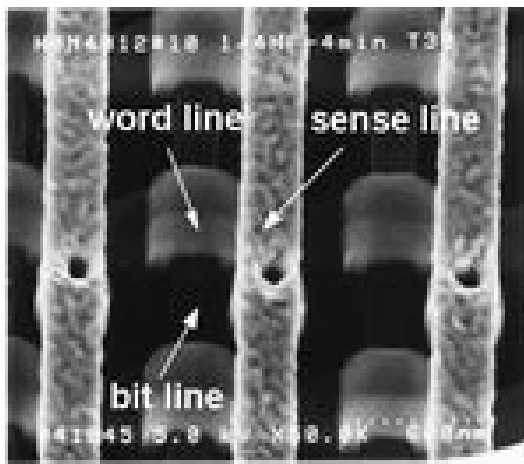
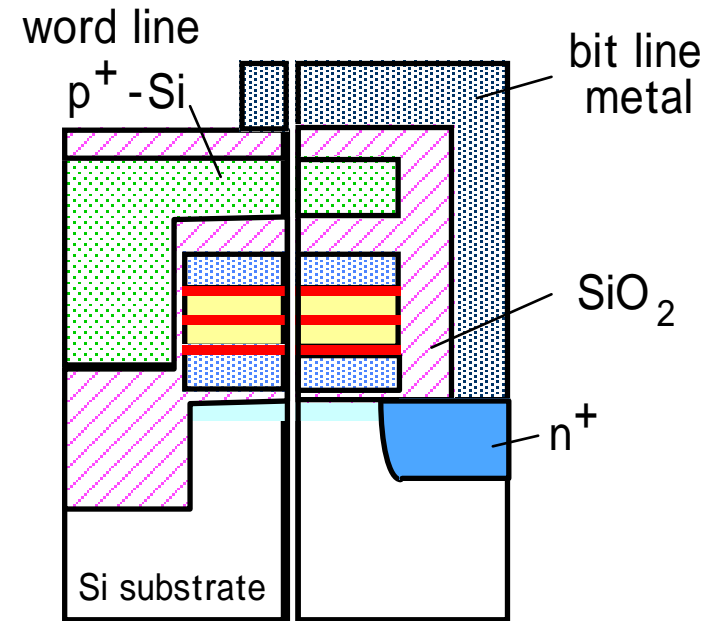
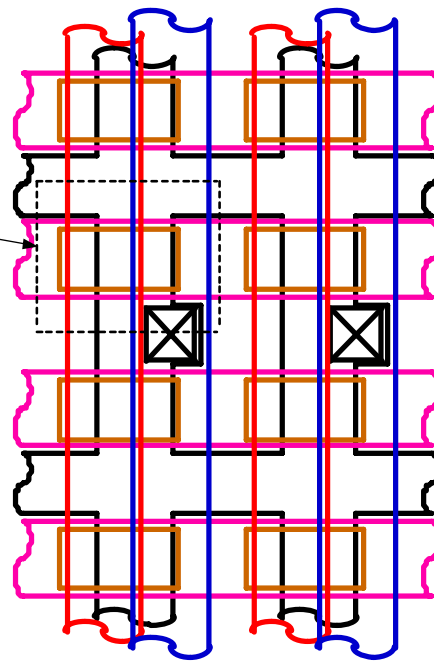


# Memory Cell Layout

Unit cell  
 $2.5F \times 2F = 5F^2$

⇕

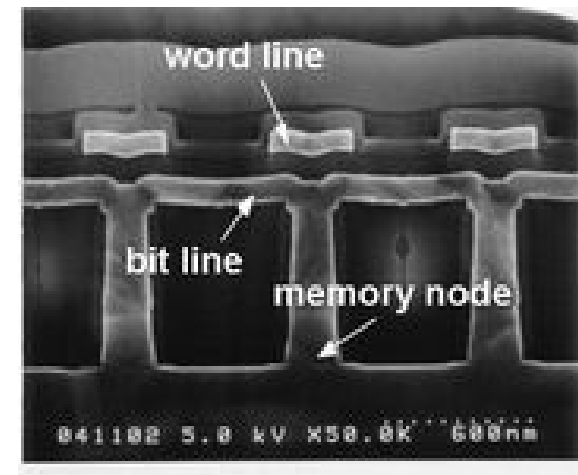
DRAM 1-T cell  
 $6-8F^2$



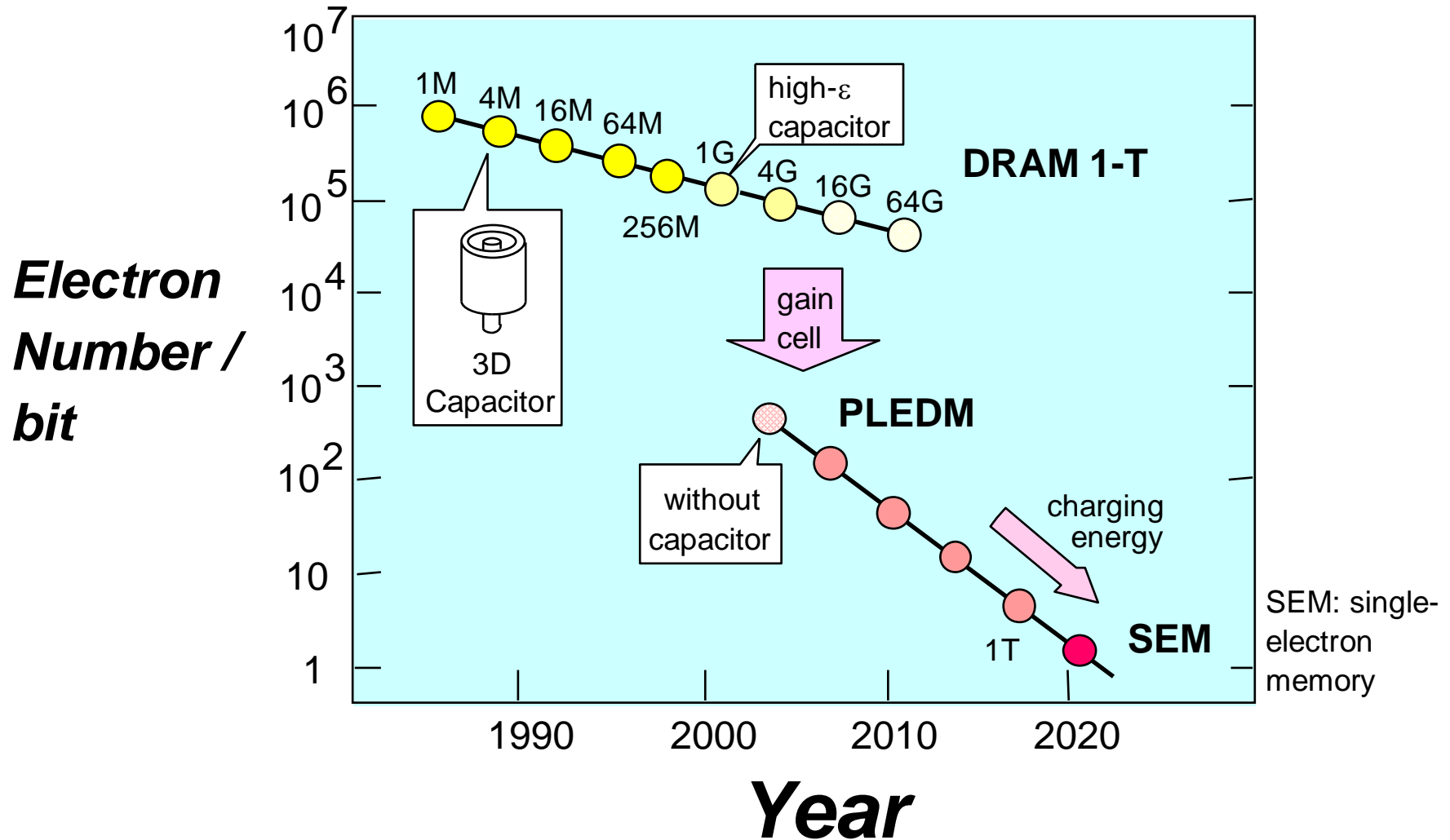
plan view



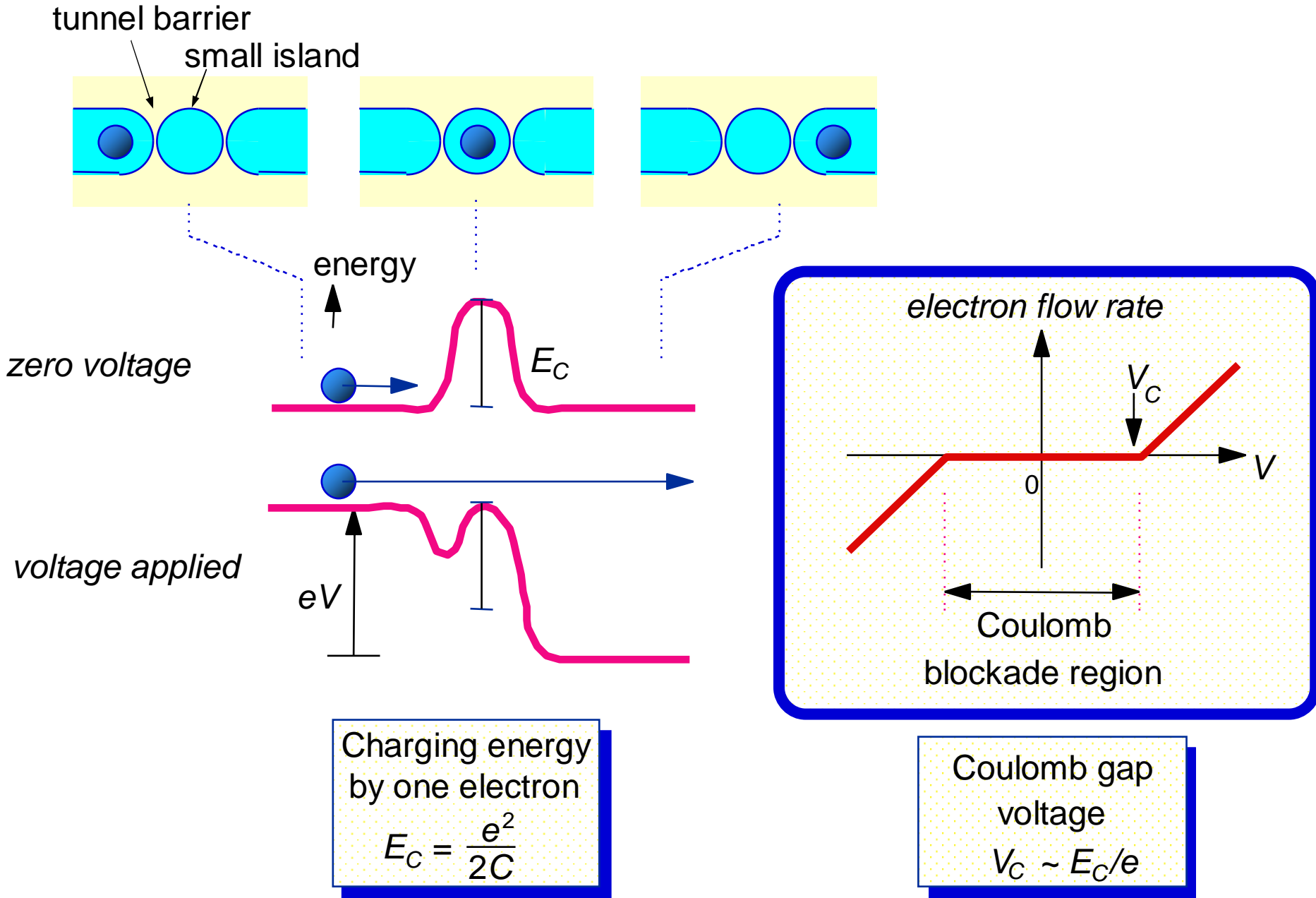
cross sectional view



# Electron Number Stored in a Memory Cell

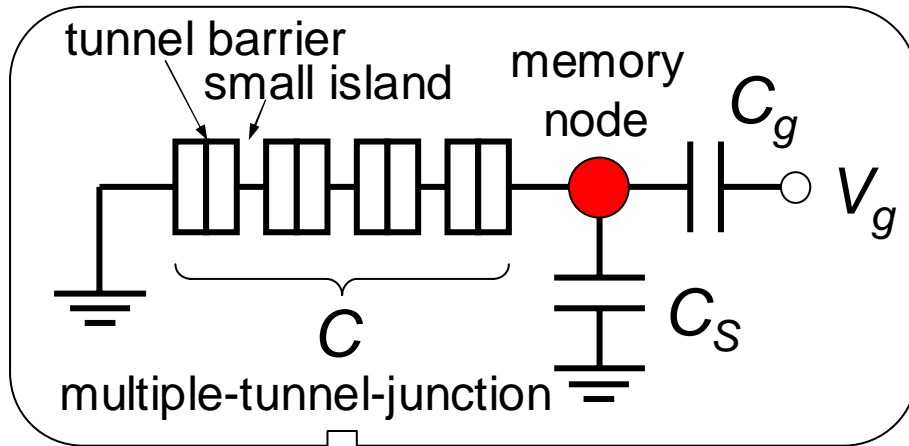


# Coulomb Blockade

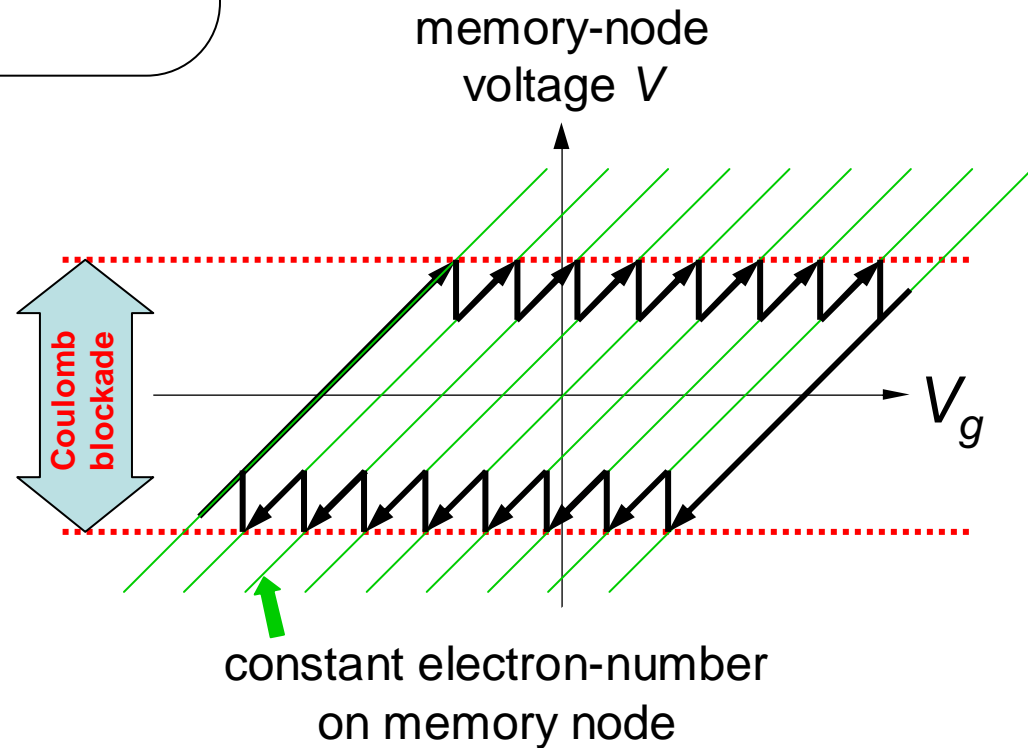
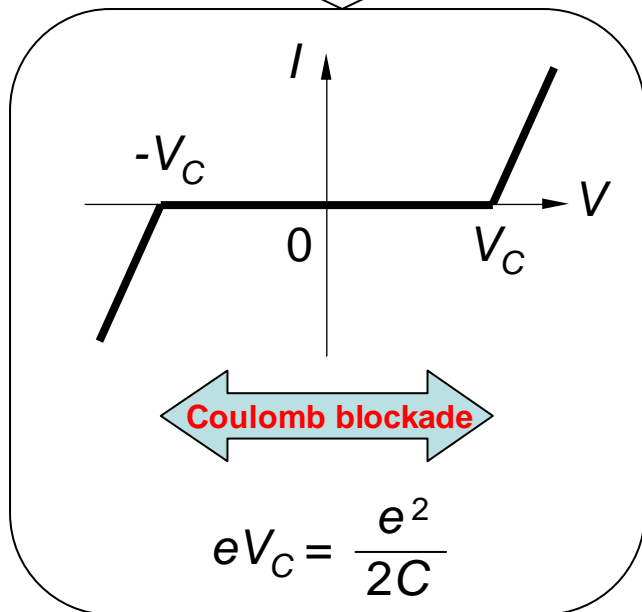




# Single-electron Memory

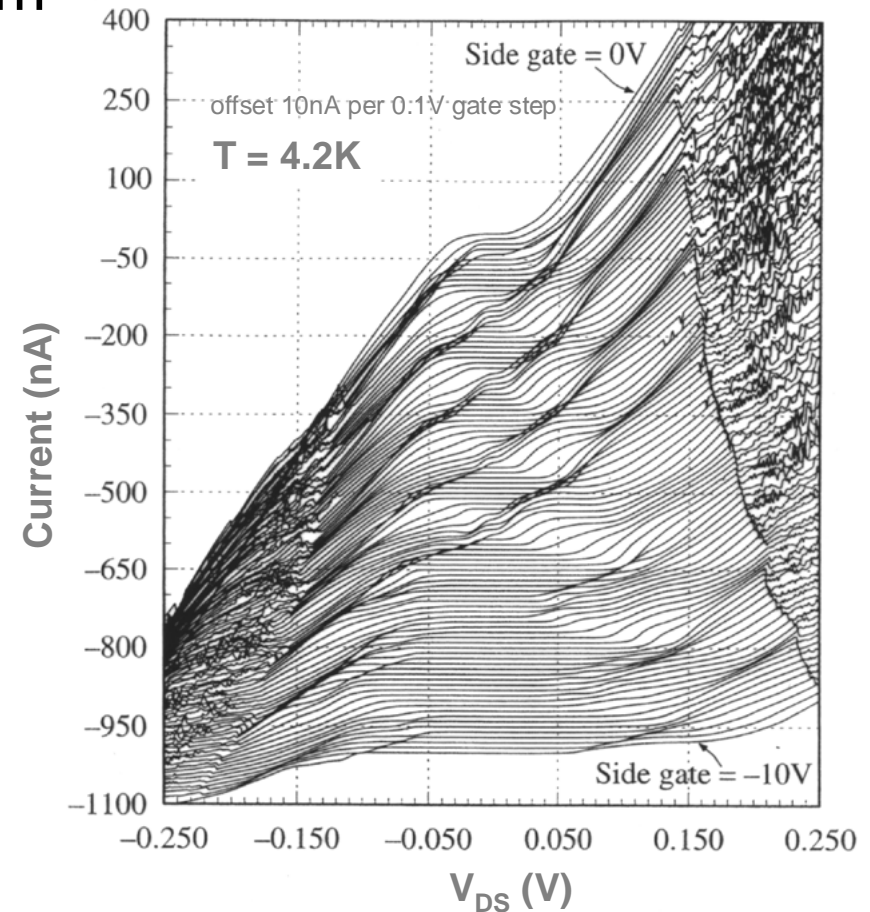
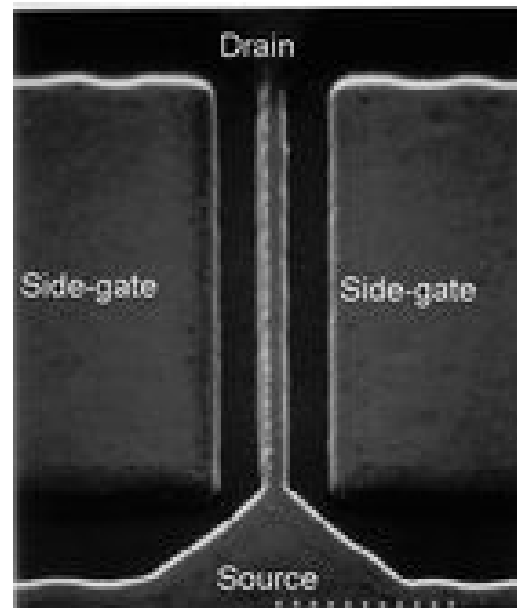
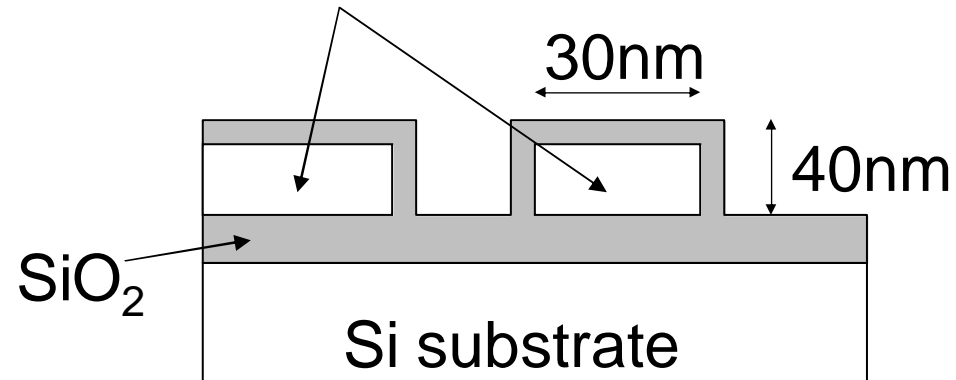


$$V = \frac{C_g V_g - e n}{C + C_g + C_S}$$

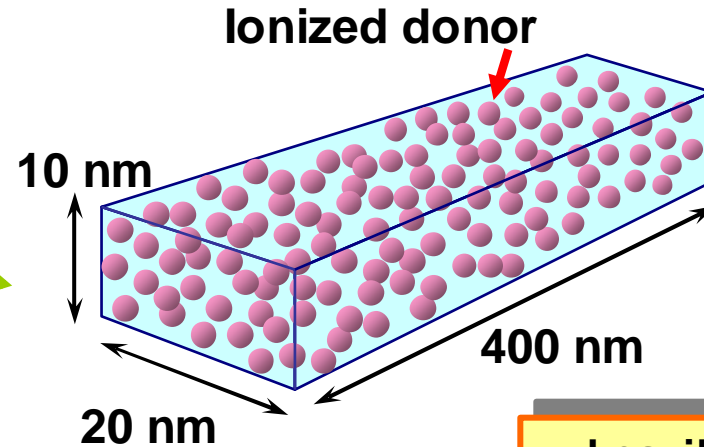
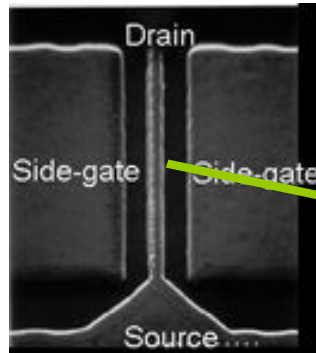


# Silicon In-plane Gate Multiple-Tunnel-Junction

Single-crystal Si, doped with P  $10^{19}\text{cm}^{-3}$



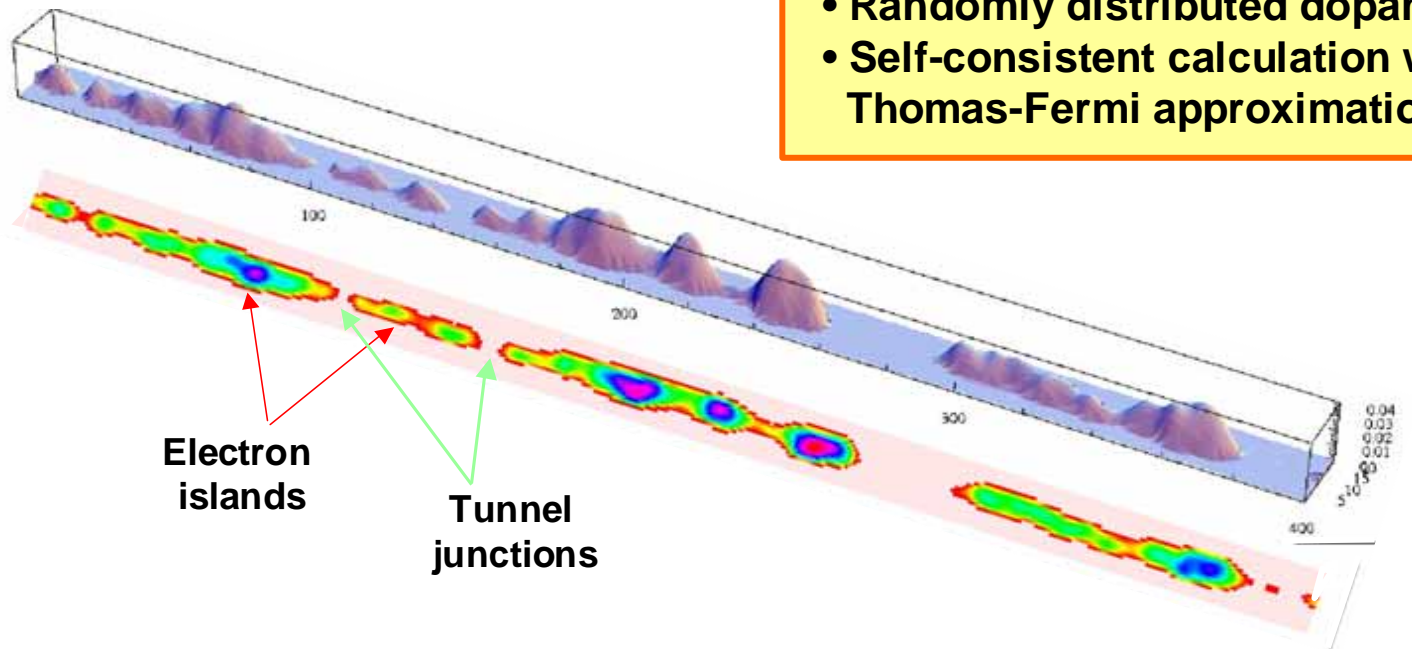
# Naturally formed Electron Islands



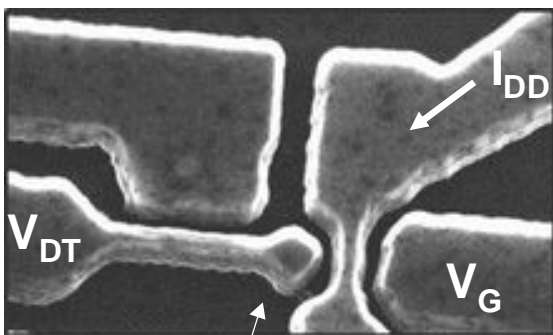
R. J. Blaikie, K. Nakazato, R. B. S. Oakeshott, J. R. A. Cleaver, and H. Ahmed, *Appl. Phys. Lett.* **64**, pp. 118-120 (1994)

G. J. Evans, H. Mizuta, and H. Ahmed, *Jpn. J. Appl. Phys.* **40**, pp. 5837-5840 (2001)

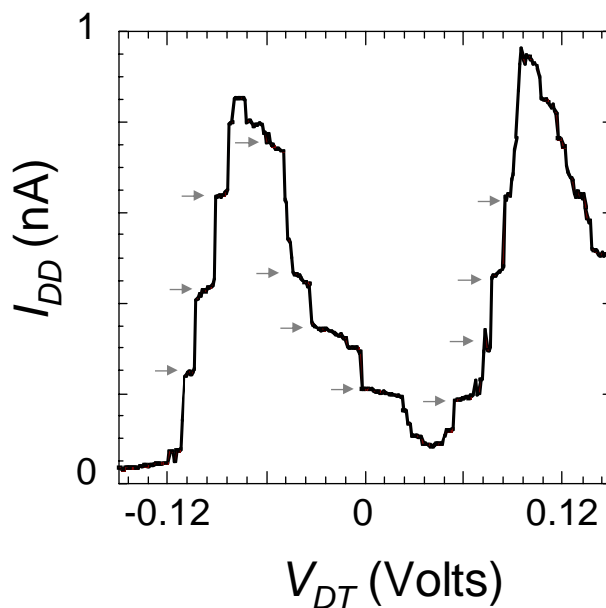
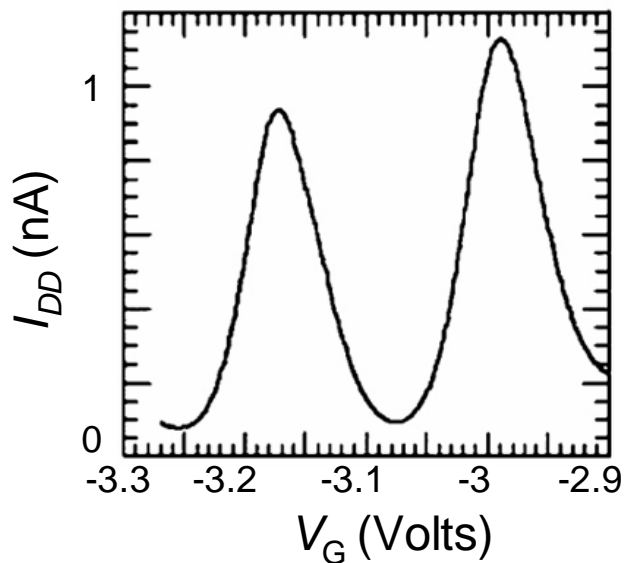
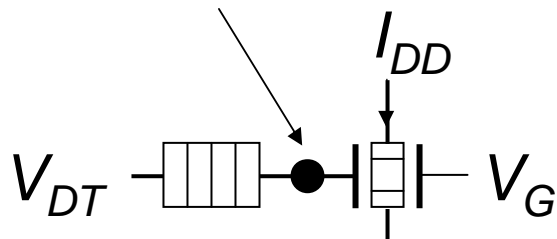
- heavily doped silicon nanowire
- Randomly distributed dopants
- Self-consistent calculation with Thomas-Fermi approximation



# Si Single-electron Memory

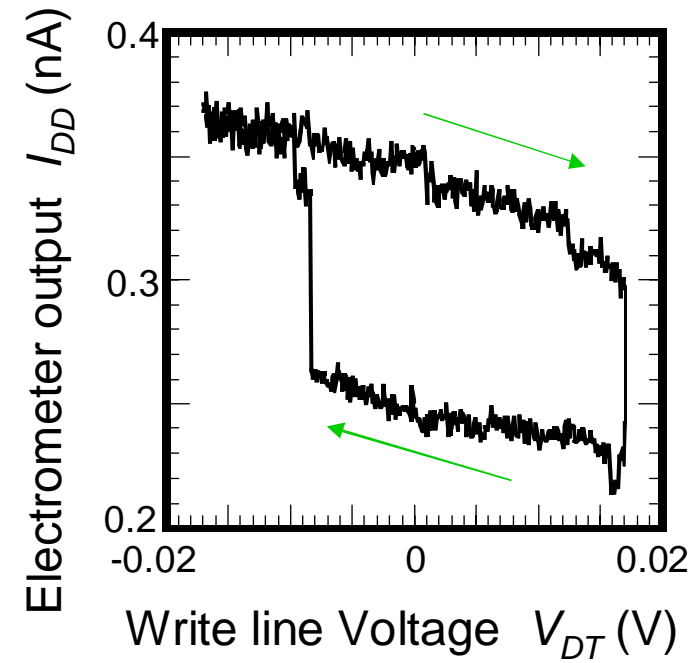
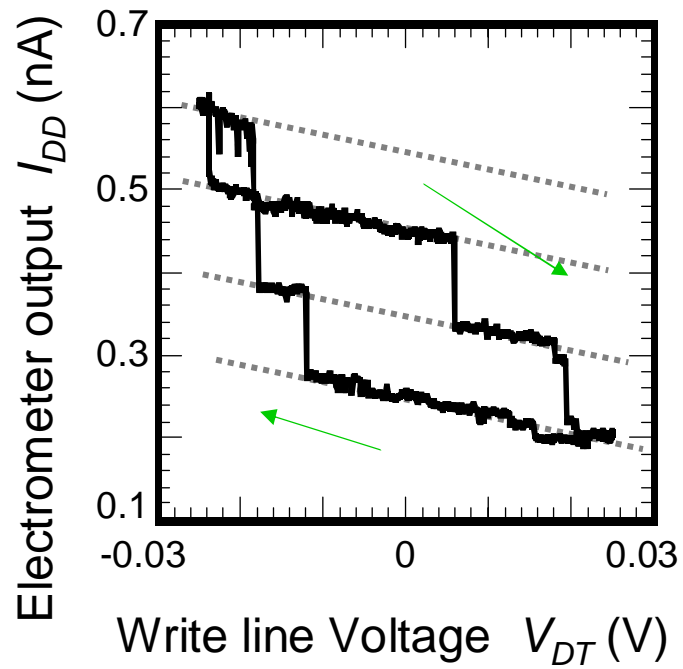


electron storage node  
< 30nm

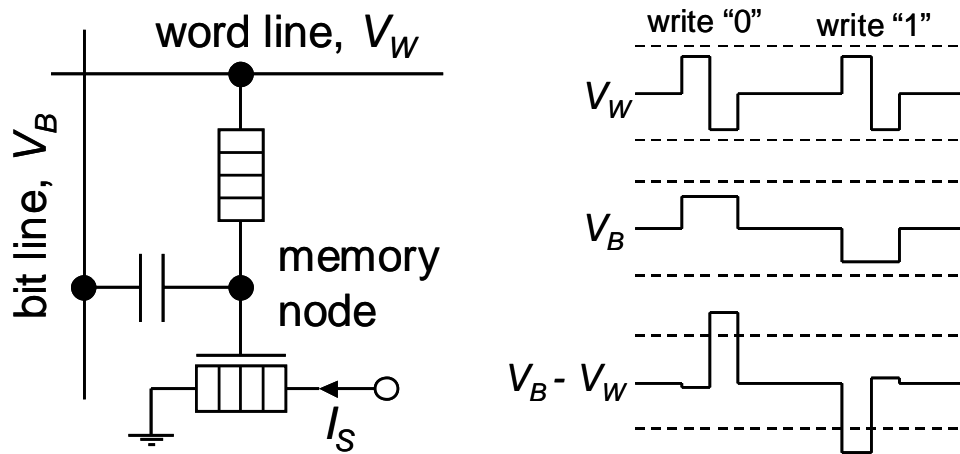


N. J. Stone and H. Ahmed,  
*Appl. Phys. Lett.* **77**, pp. 744-746 (2000)

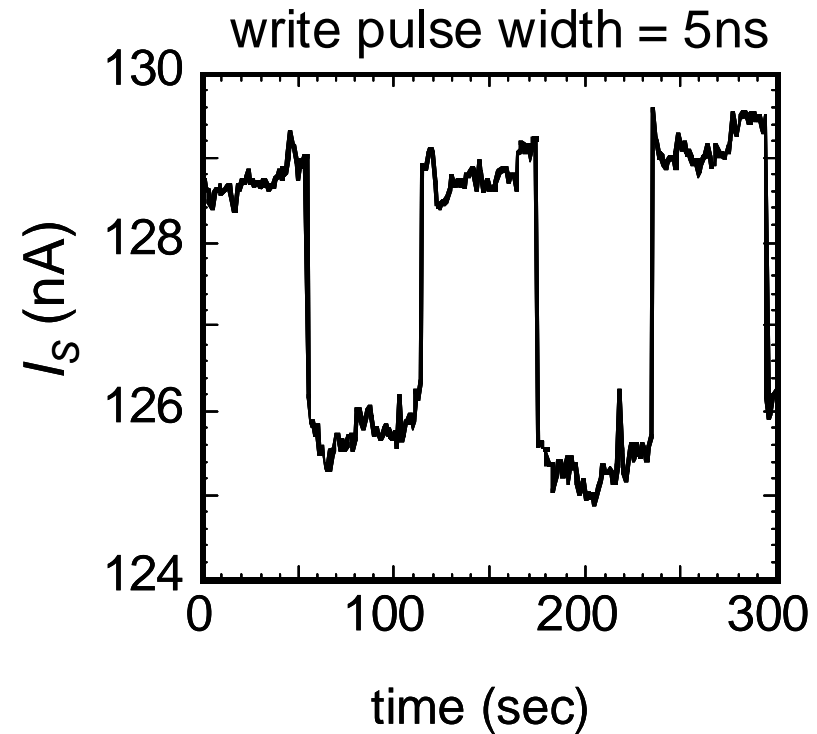
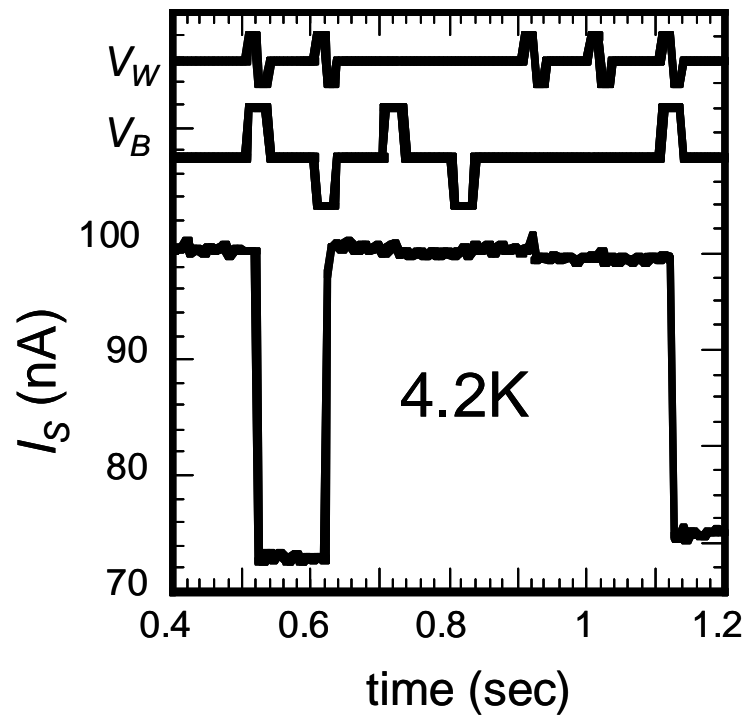
***one bit = one electron***



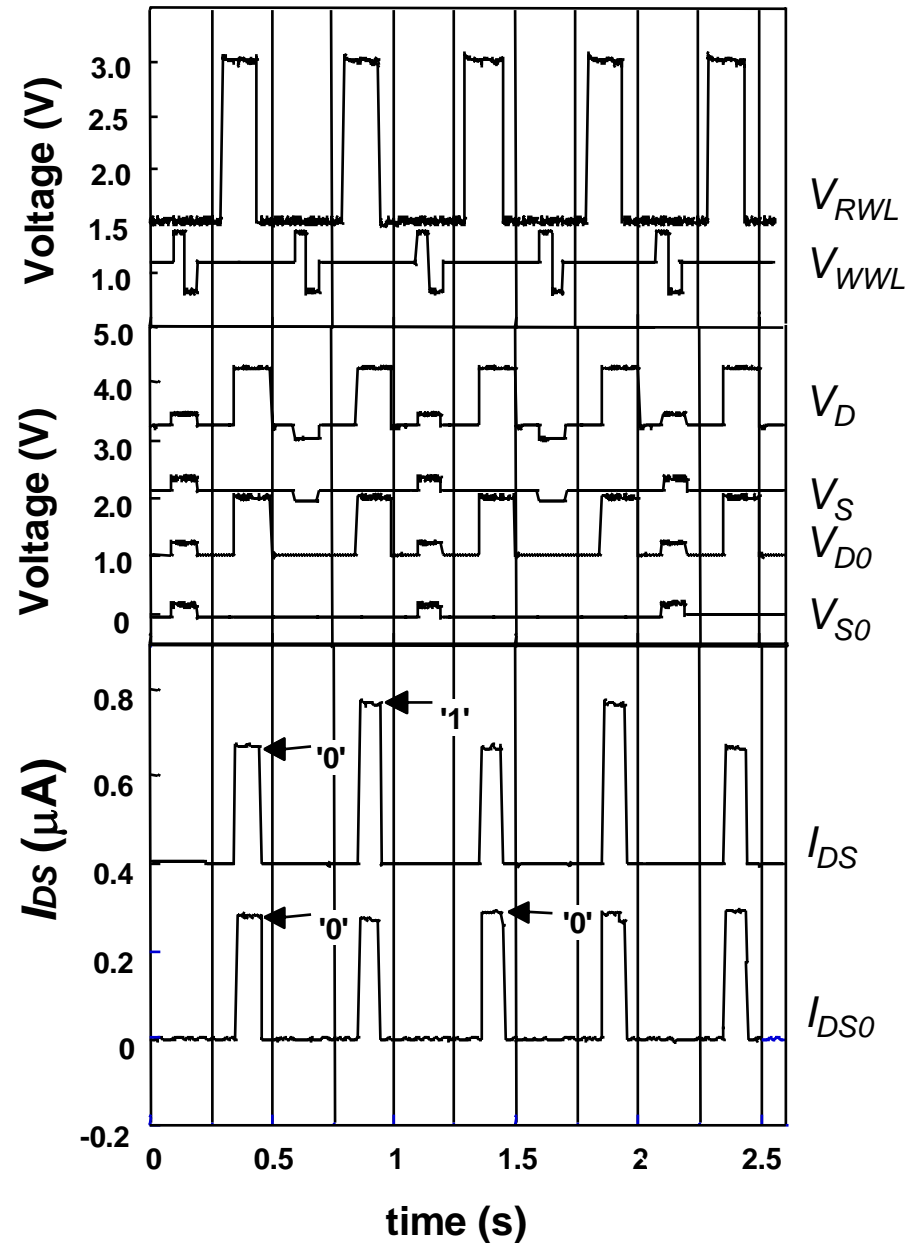
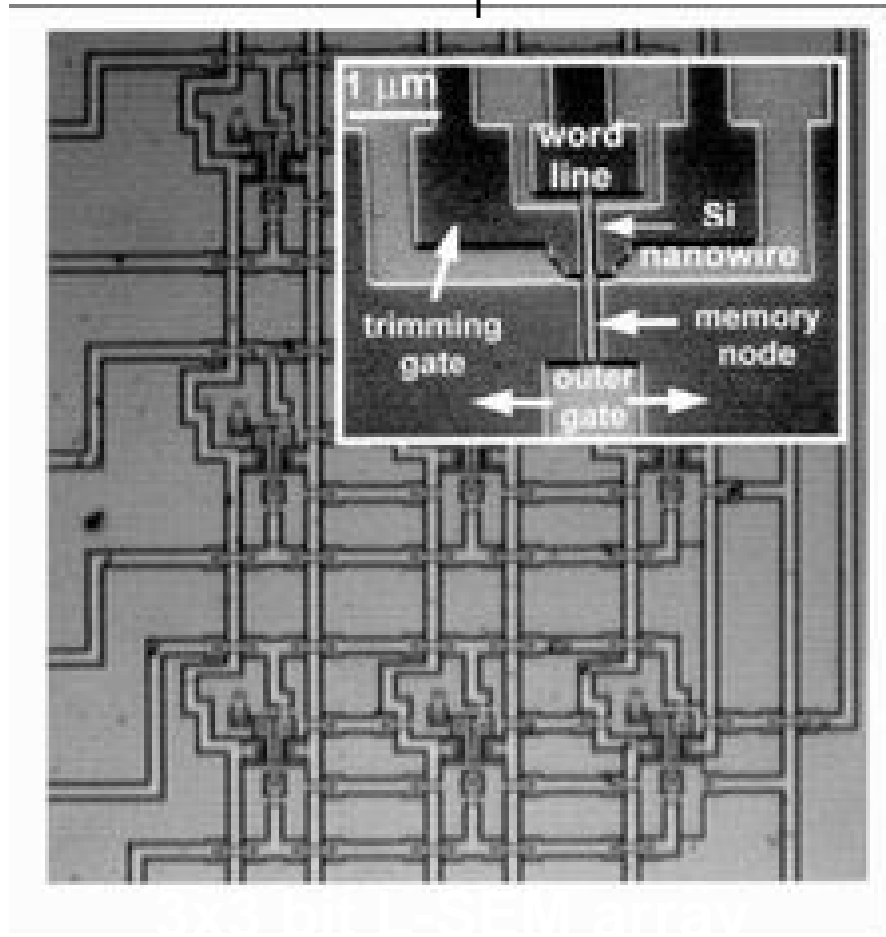
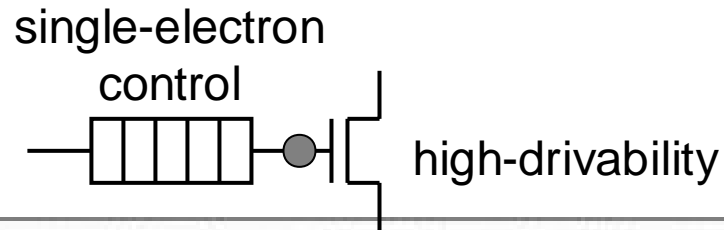
# Random Write to Single-electron Memory Cell Array



N J Stone, H Ahmed, and K Nakazato,  
*IEEE EDL* **20**, pp. 583-585, 1999

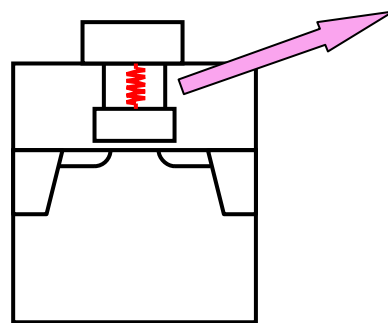
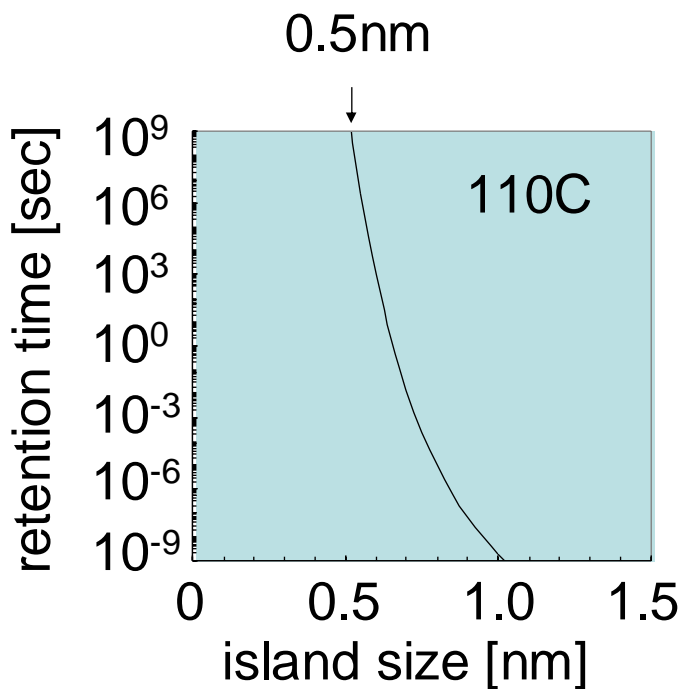


# Single-electron Transistor – CMOS Hybrid Memory Array

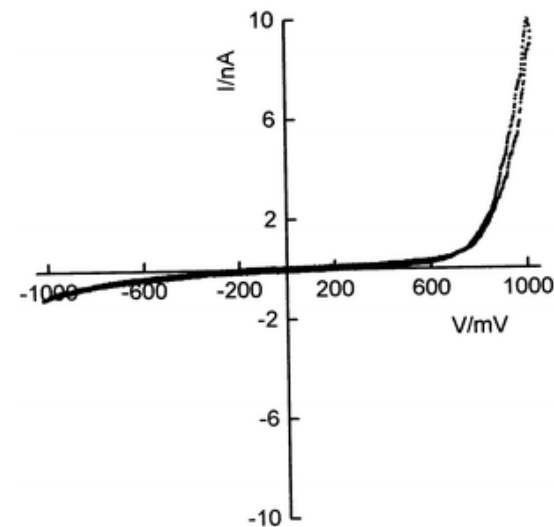
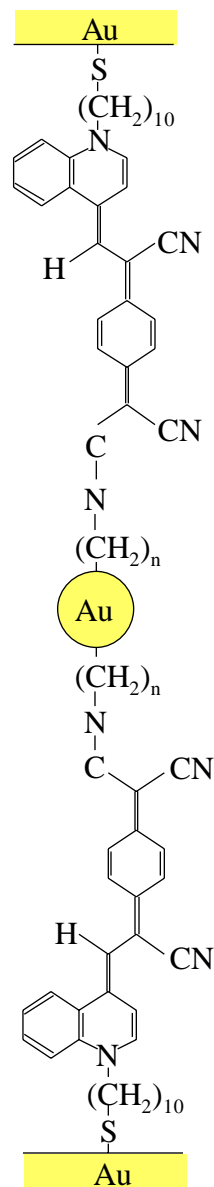


Z. A. K. Durrani, A. C. Irvine, H. Ahmed, and K. Nakazato,  
*Appl. Phys. Lett.* **74**, pp. 1293-1295 (1999)

# Molecular Single-electron Memory



Molecular single-electron memory



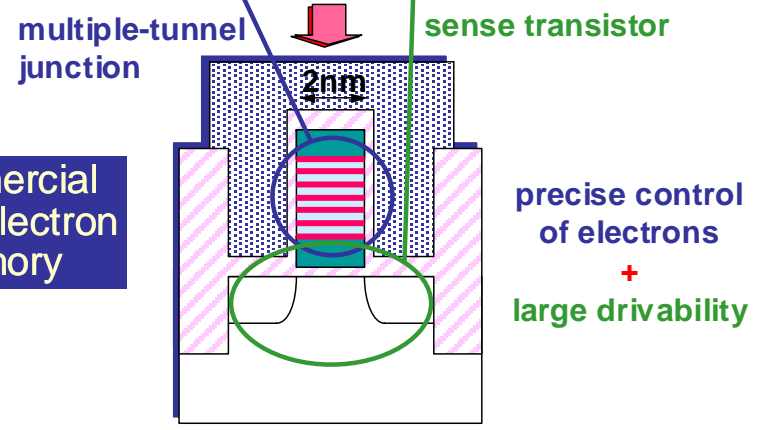
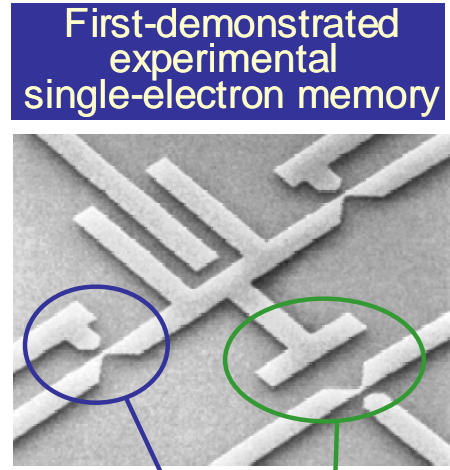
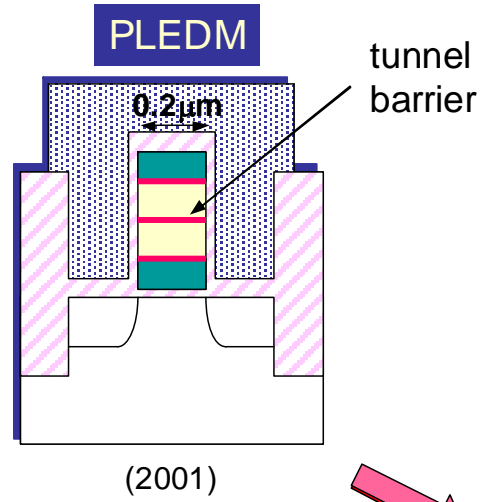
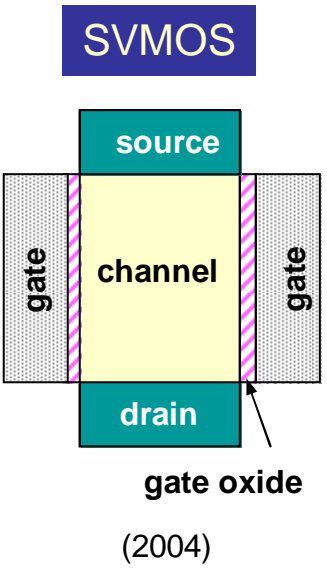
Current-voltage characteristics of a self-assembled monolayer on a gold-coated substrate and investigated using a decanethiol-coated gold tip.

Self-assembled monolayer donor-( $\pi$ -bridge)-acceptor dye

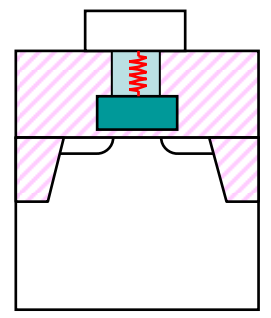
Collaboration with Cranfield University, U.K.



# Summary



**commercial single-electron memory**



**molecular single-electron memory**