

Lost 20-years Since 1990 Semiconductor in Japan Today, Yesterday, and Then Future

Takayuki Ohba
The Univ. of Tokyo

Memory and Logic
1Tb/cm²

WOW
Alliance

WOW 3D Integration Technology

Realizing **U**nlimited **U**LSIs

Bumpless and Dual-Damascene Via-Last after Bonding

Ultra-Thinned Wafer Back-to-Front Stack

The University of Tokyo, Ohba Lab, WOW Alliance, and WOW Research Center

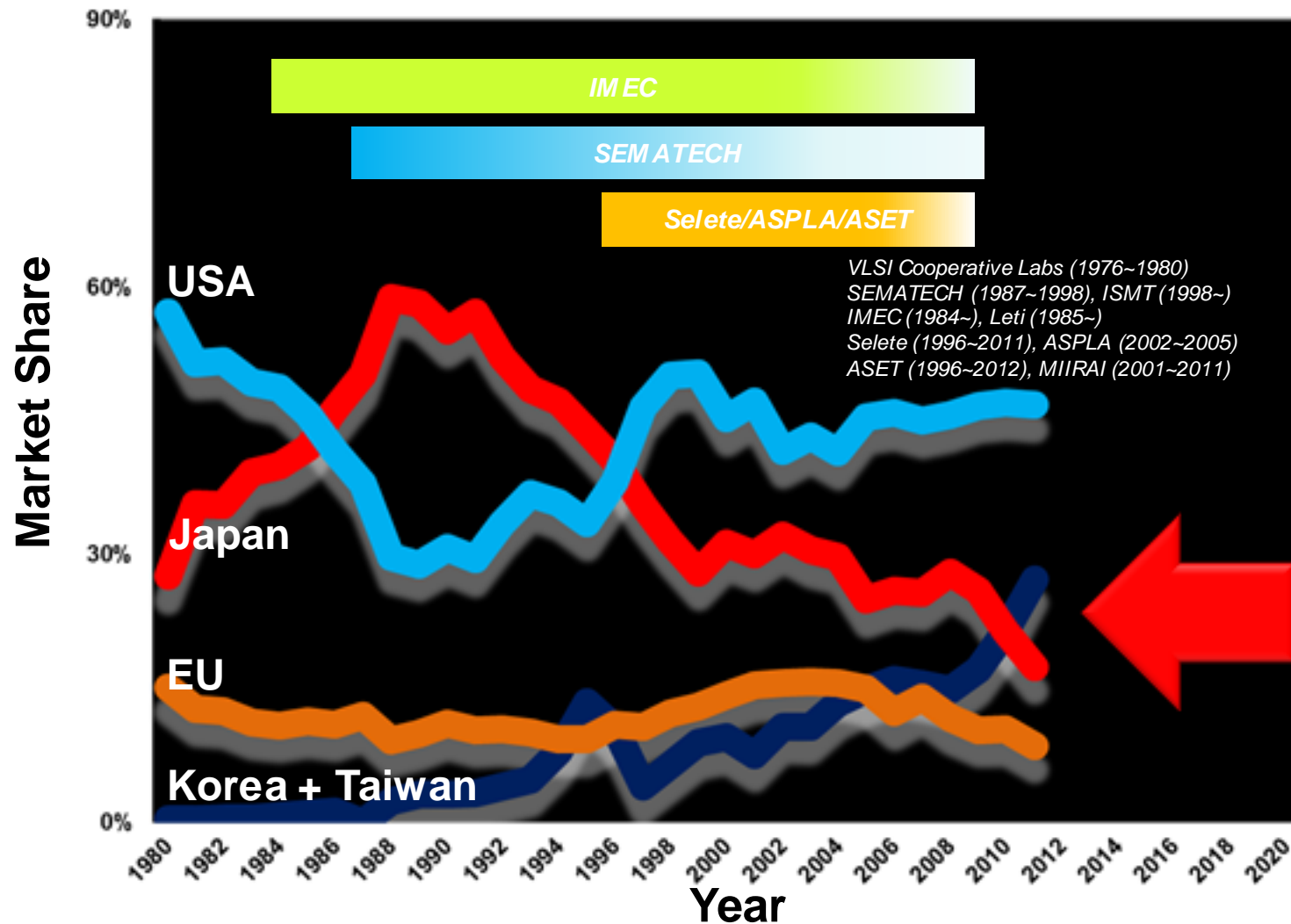


Today

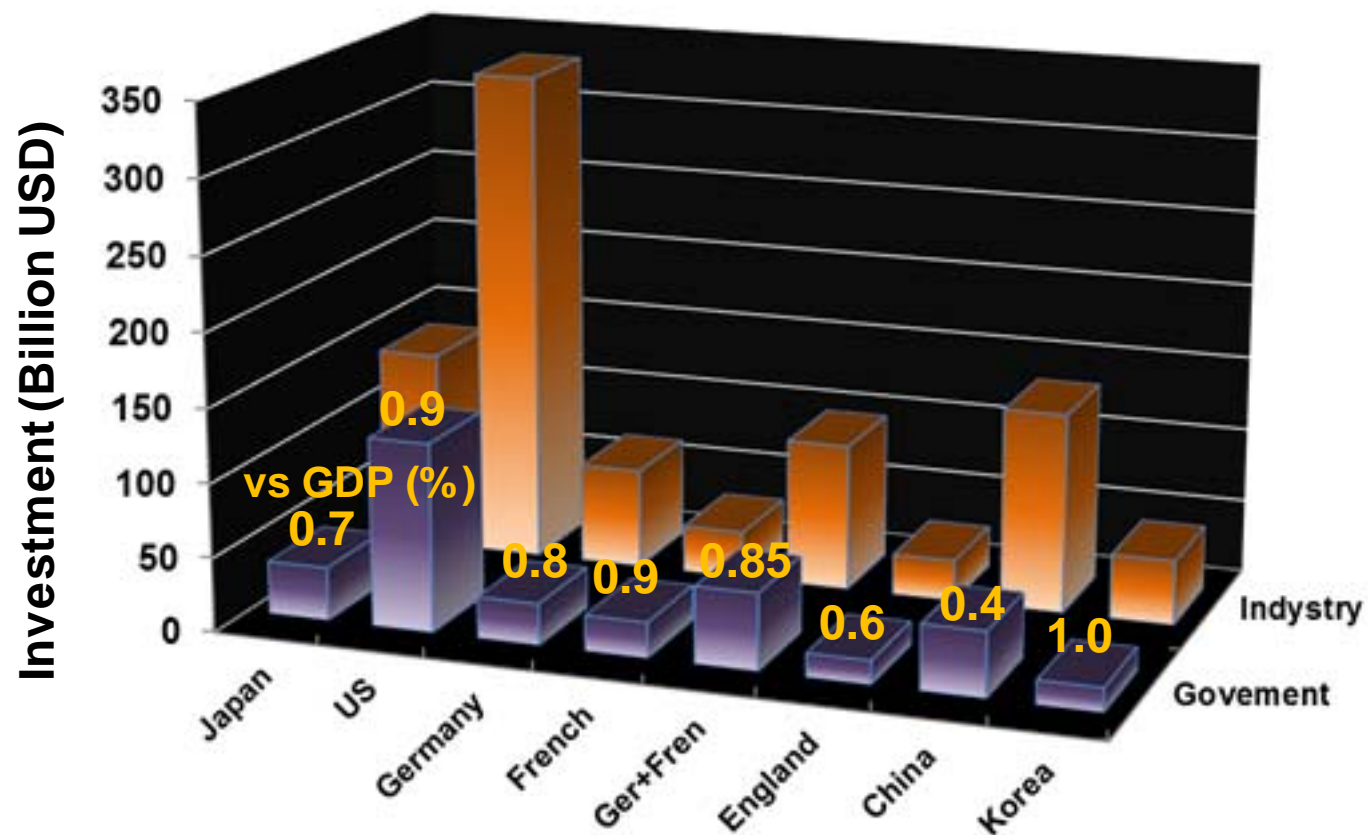
Yesterday



Yesterday, Today... Market share in Semiconductor

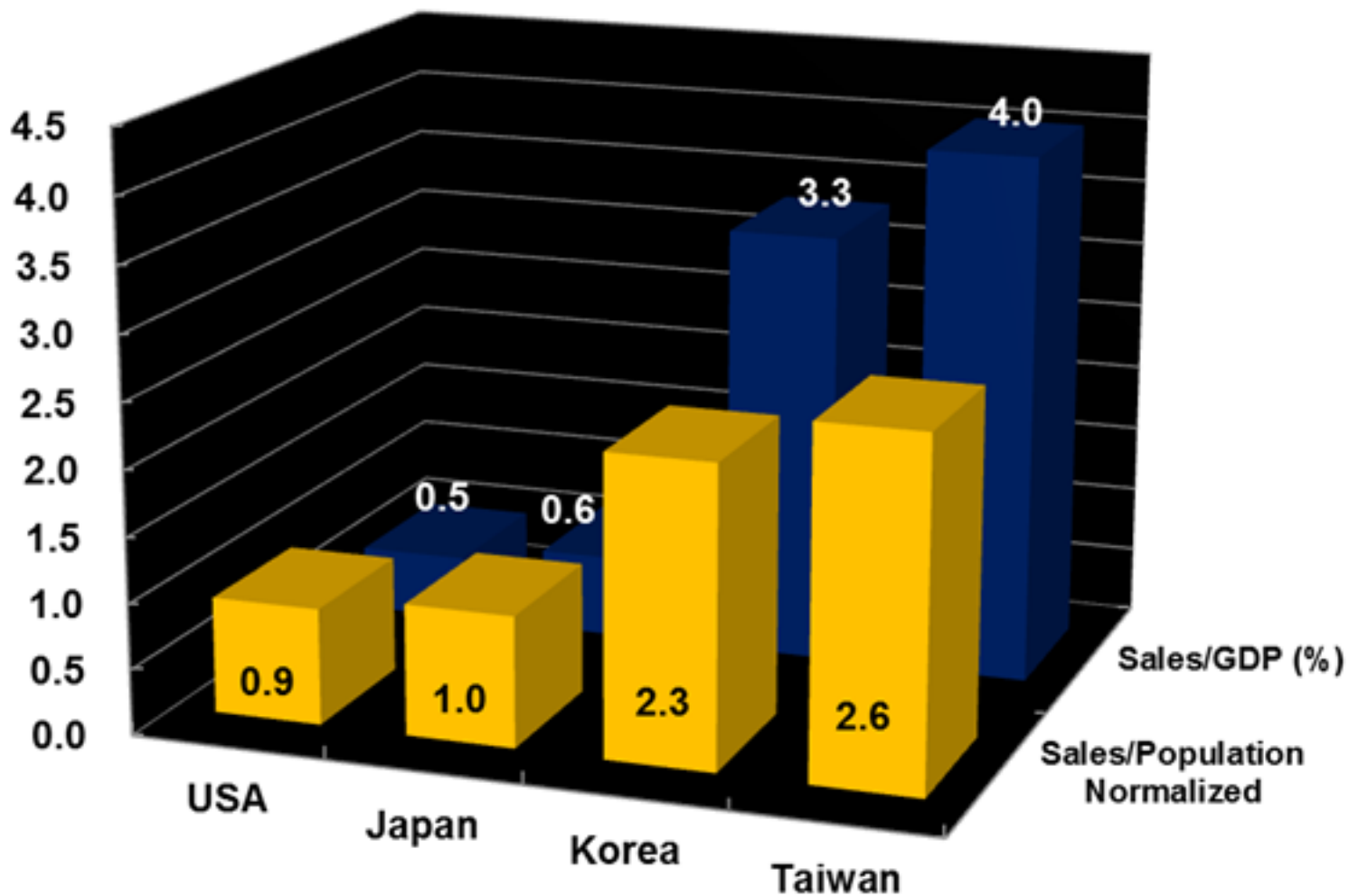


Comparison on WW R&D Budget



Source: after Nikkei April 23, 2012
 Estimated by 2009-2010

Impact Factor of Semiconductor Industries

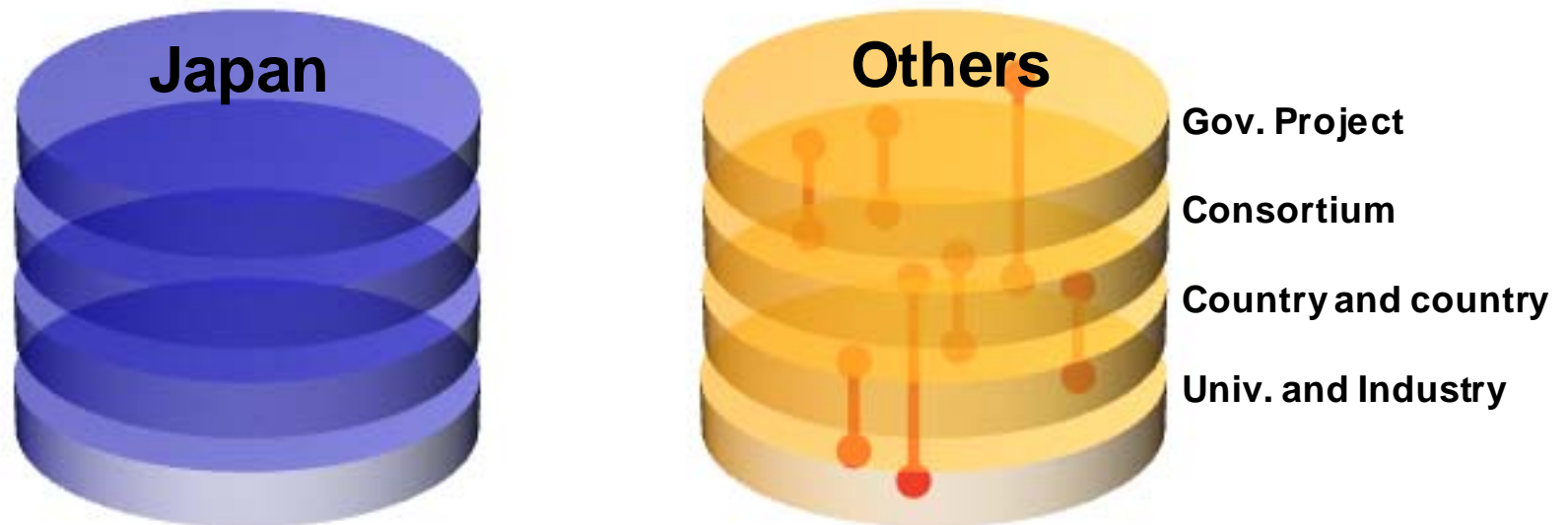


No Longer No Choice Run from Place to Place



Needs True-Integration among National Projects

Almost same research budget being provided but...

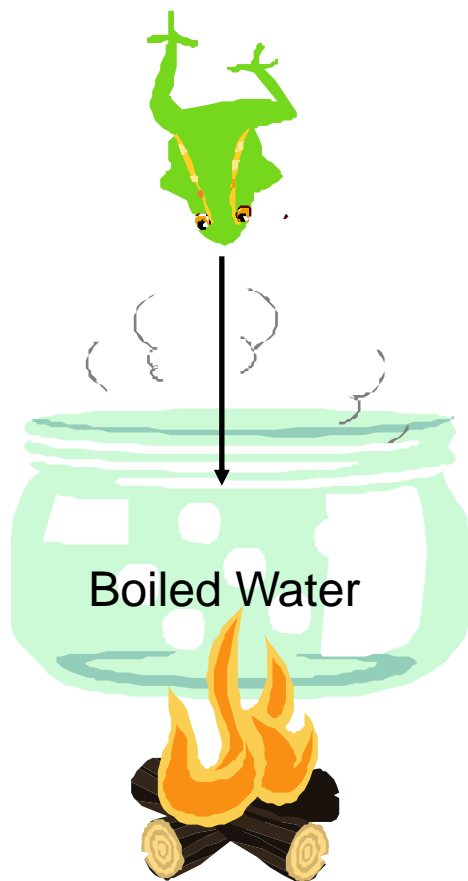


Needs Tangible Integration

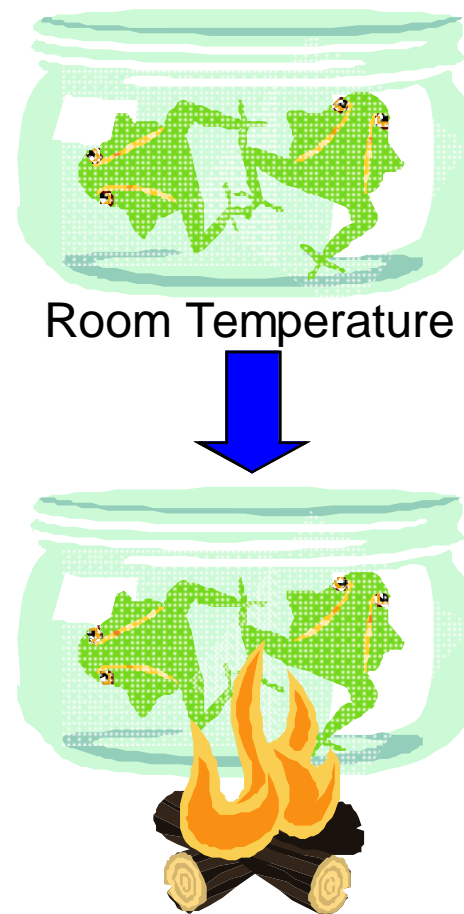
- ✓ Business oriented target
- ✓ Leadership on strong steering
- ✓ Flexible planning and attractiveness for innovation
- ✓ Global opportunities
- ✓ Short and Long term Support

How many flogs will survive?

A

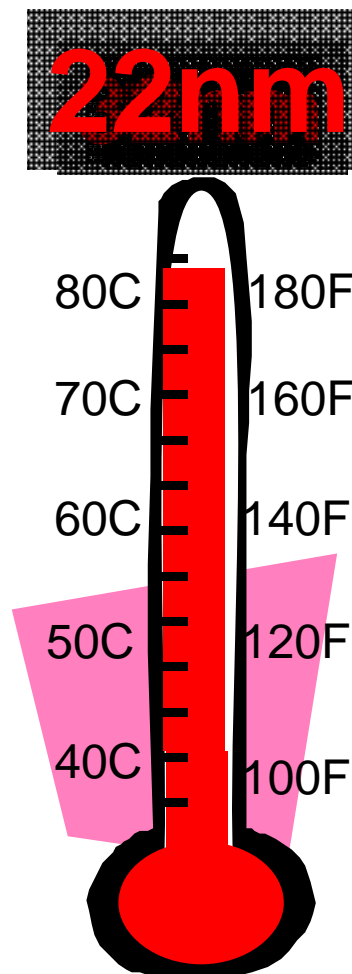
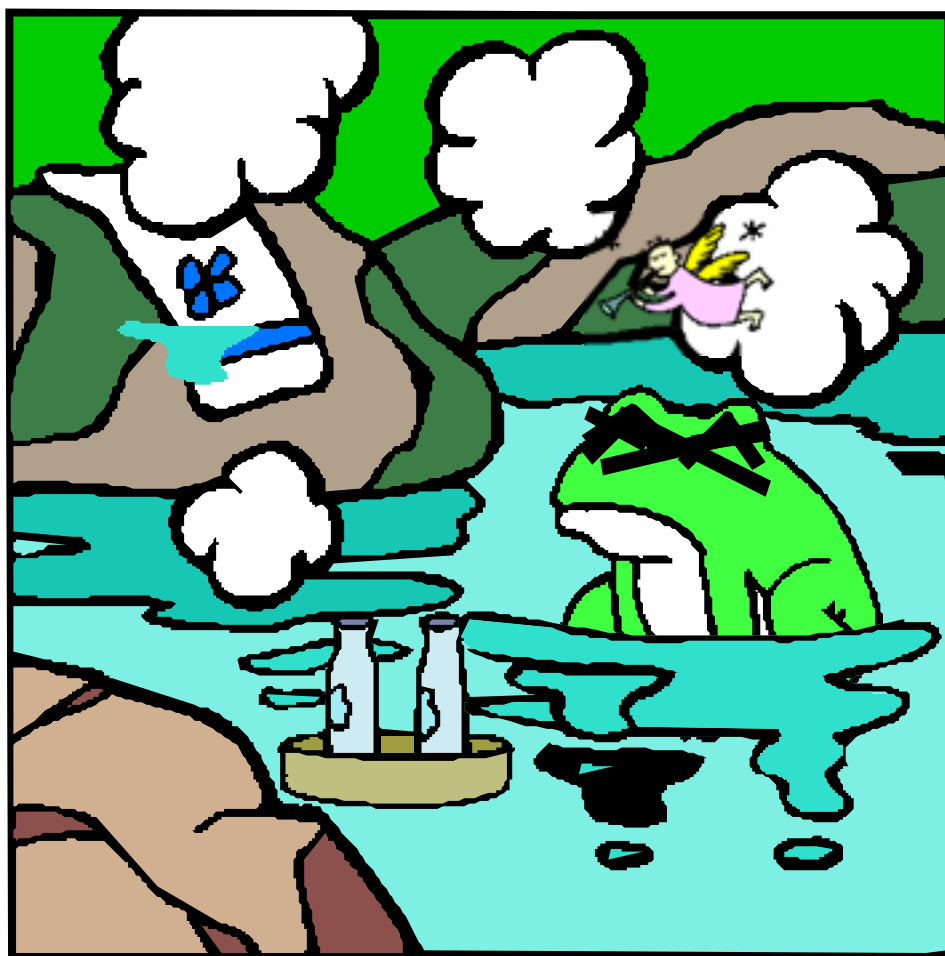


B



Big shock let them know how to survive!

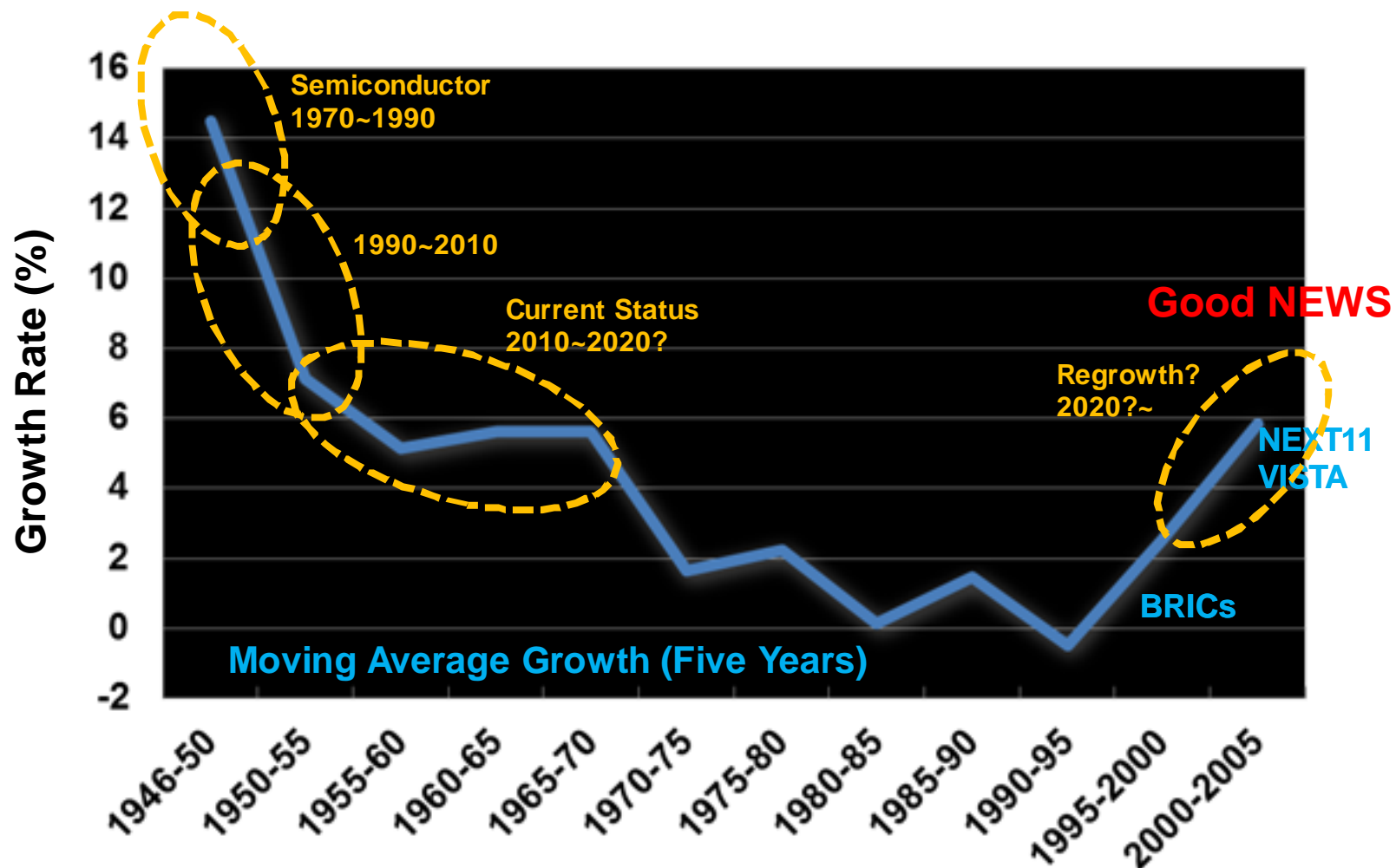
Do you want stay “Scaling Spa” any further?





Future

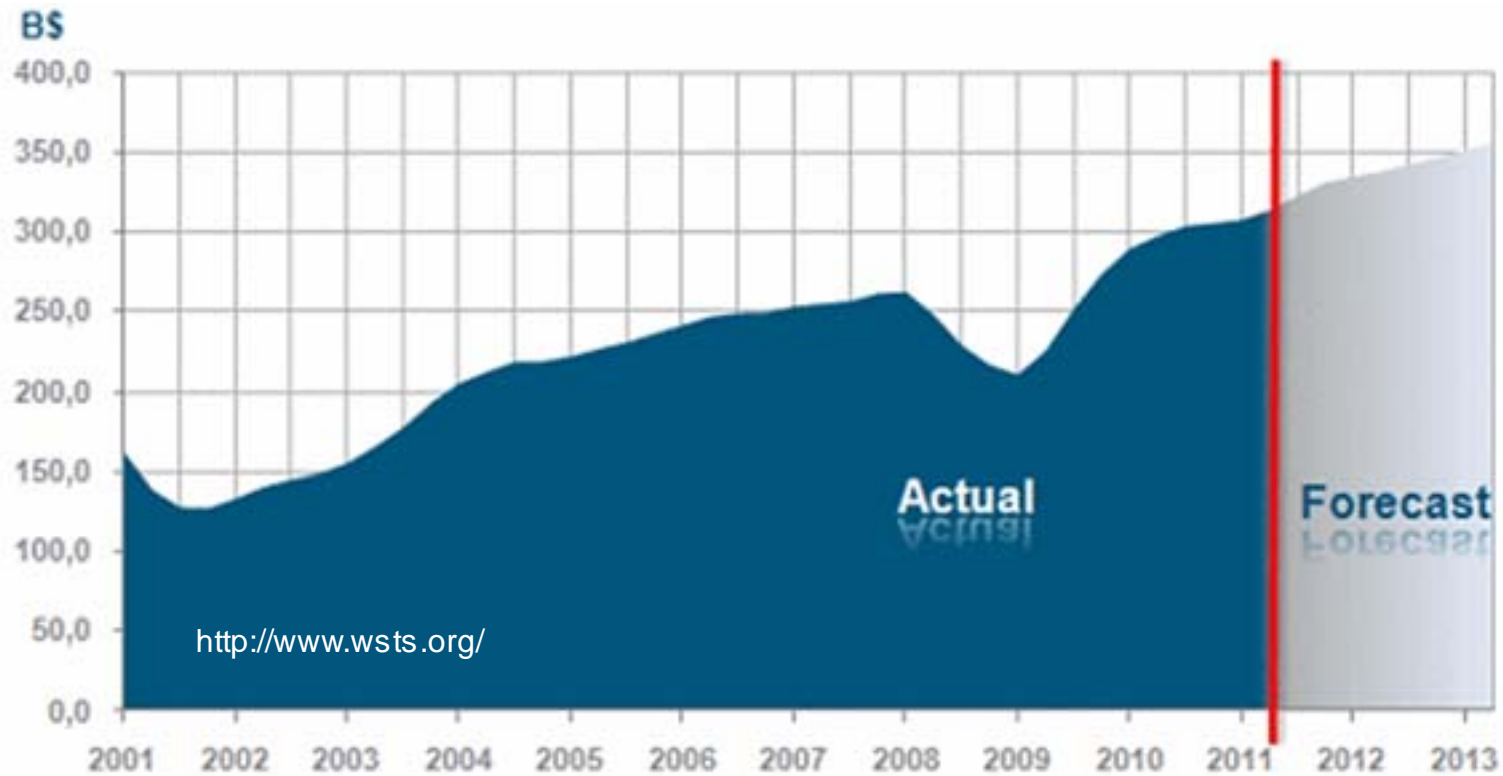
WW Steel Growth Rate



BRICs = Brazil, Russia, India, China

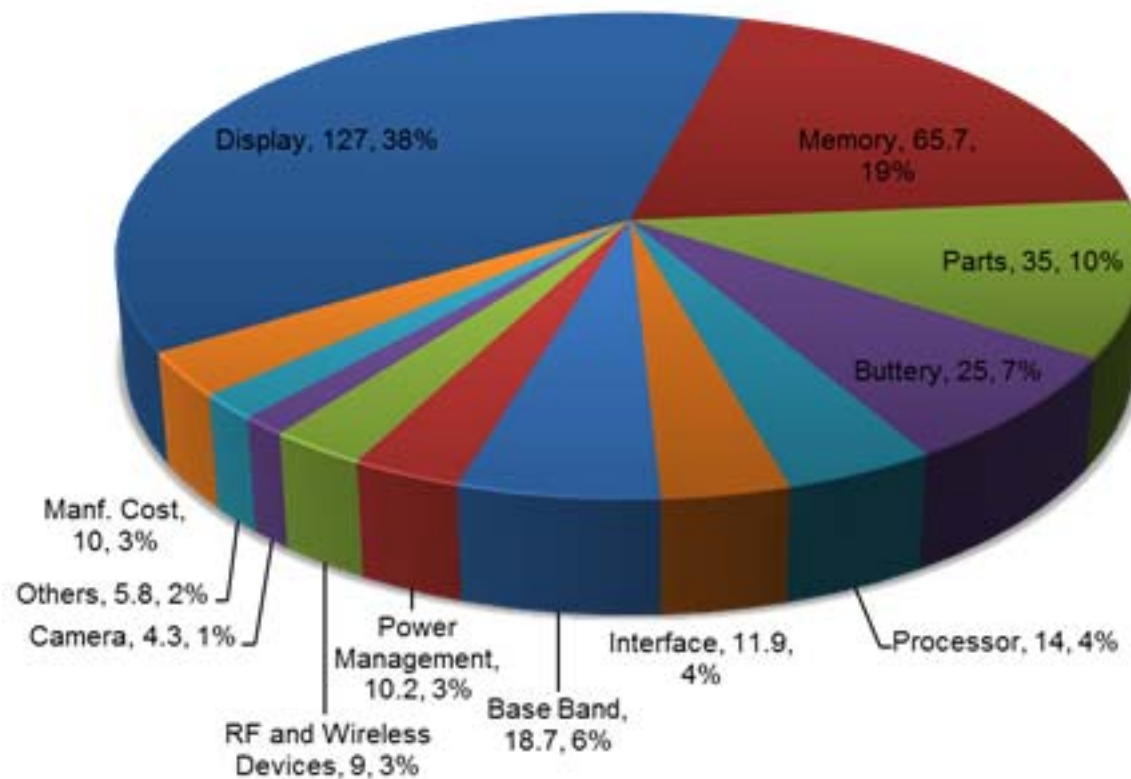
NEXT11 = Iran, Indonesia, Egypt, South Korea, Turkey, Nigeria, Pakistan, Bangladesh, Philippine, Vietnam, Mexico

WW Semiconductor Market (Billion US\$)

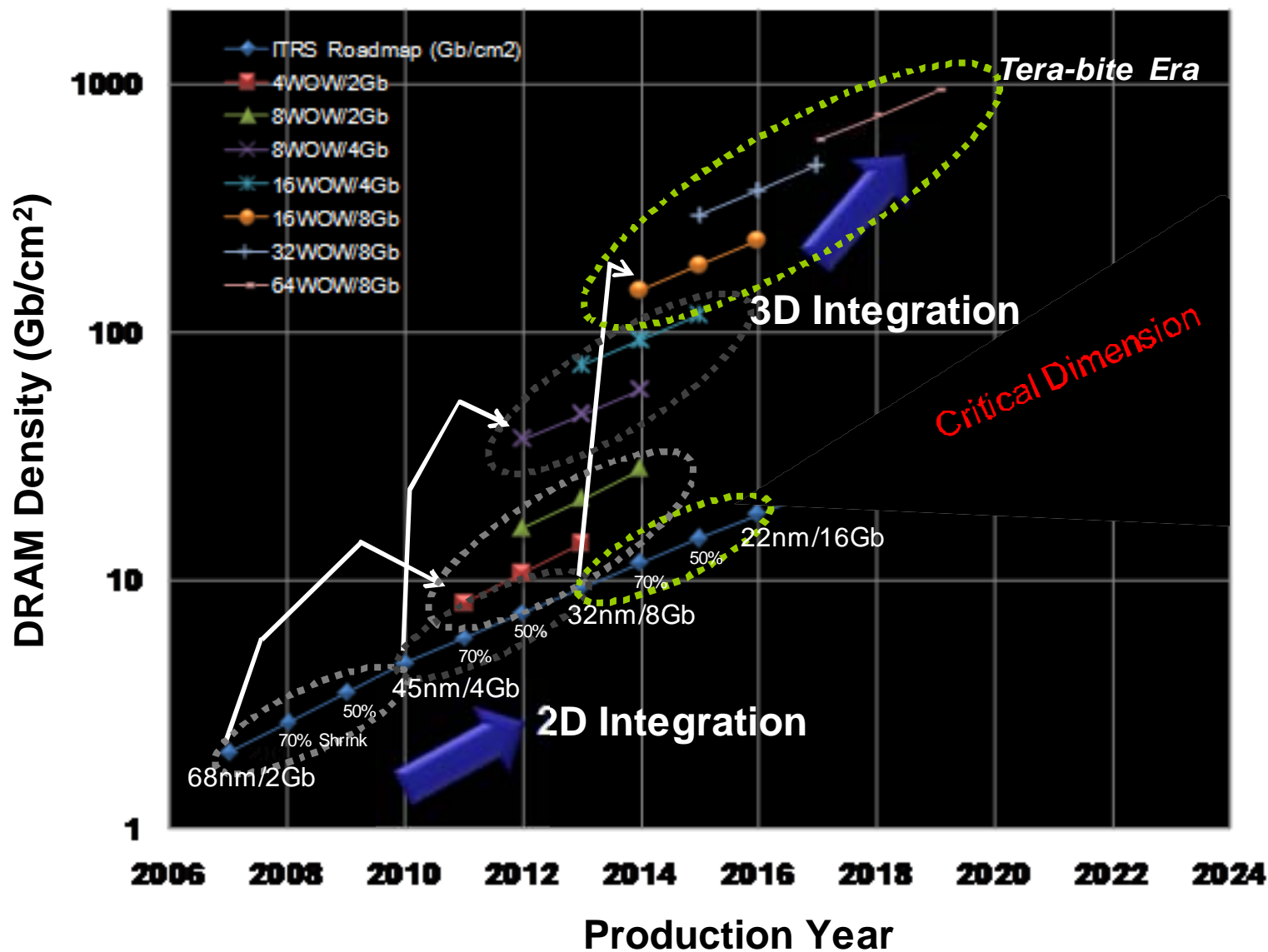


Needs more Memory/CPU/Interface Devices

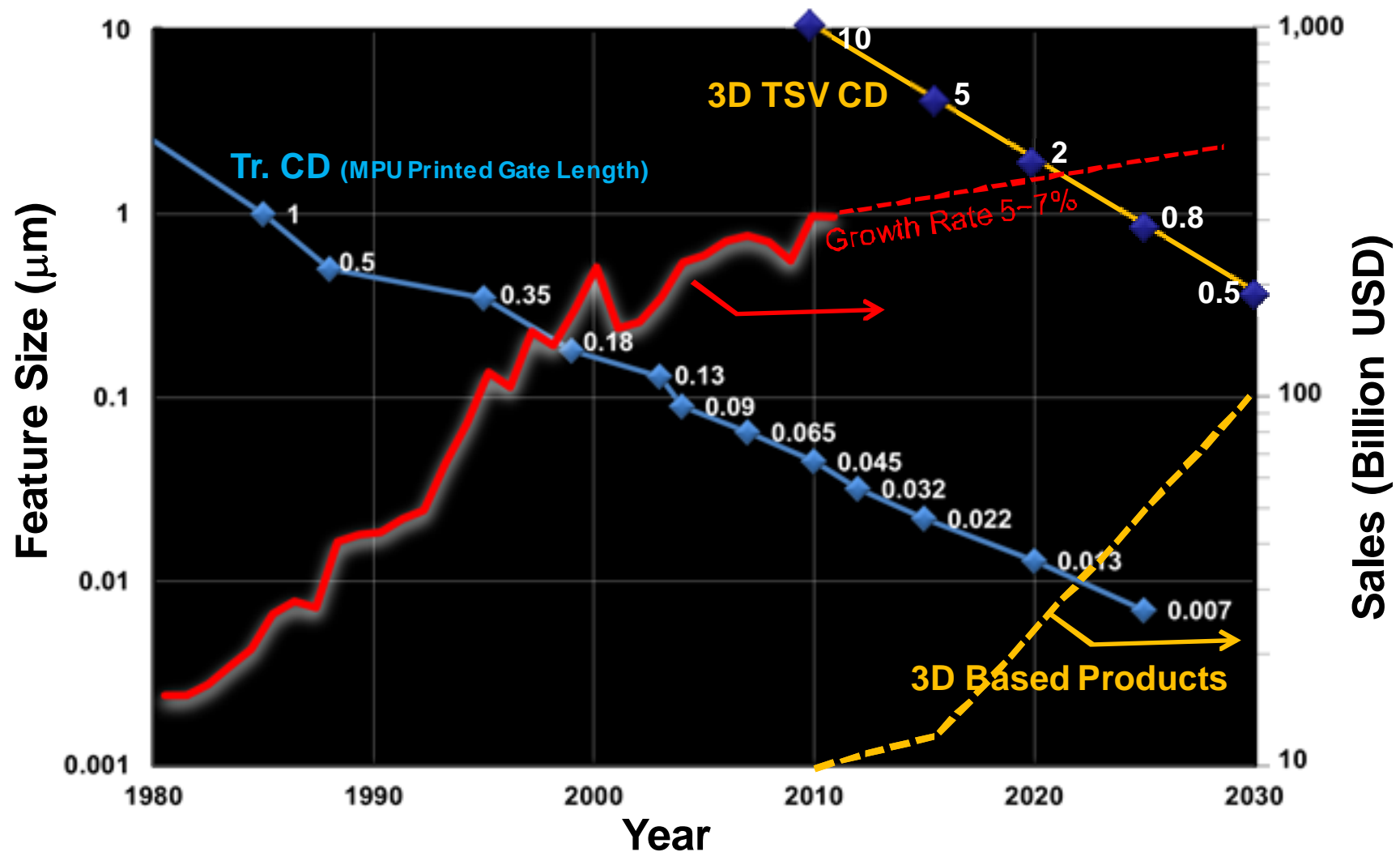
iPad2 32GB Model (USD)
Total Cost 336.6USD



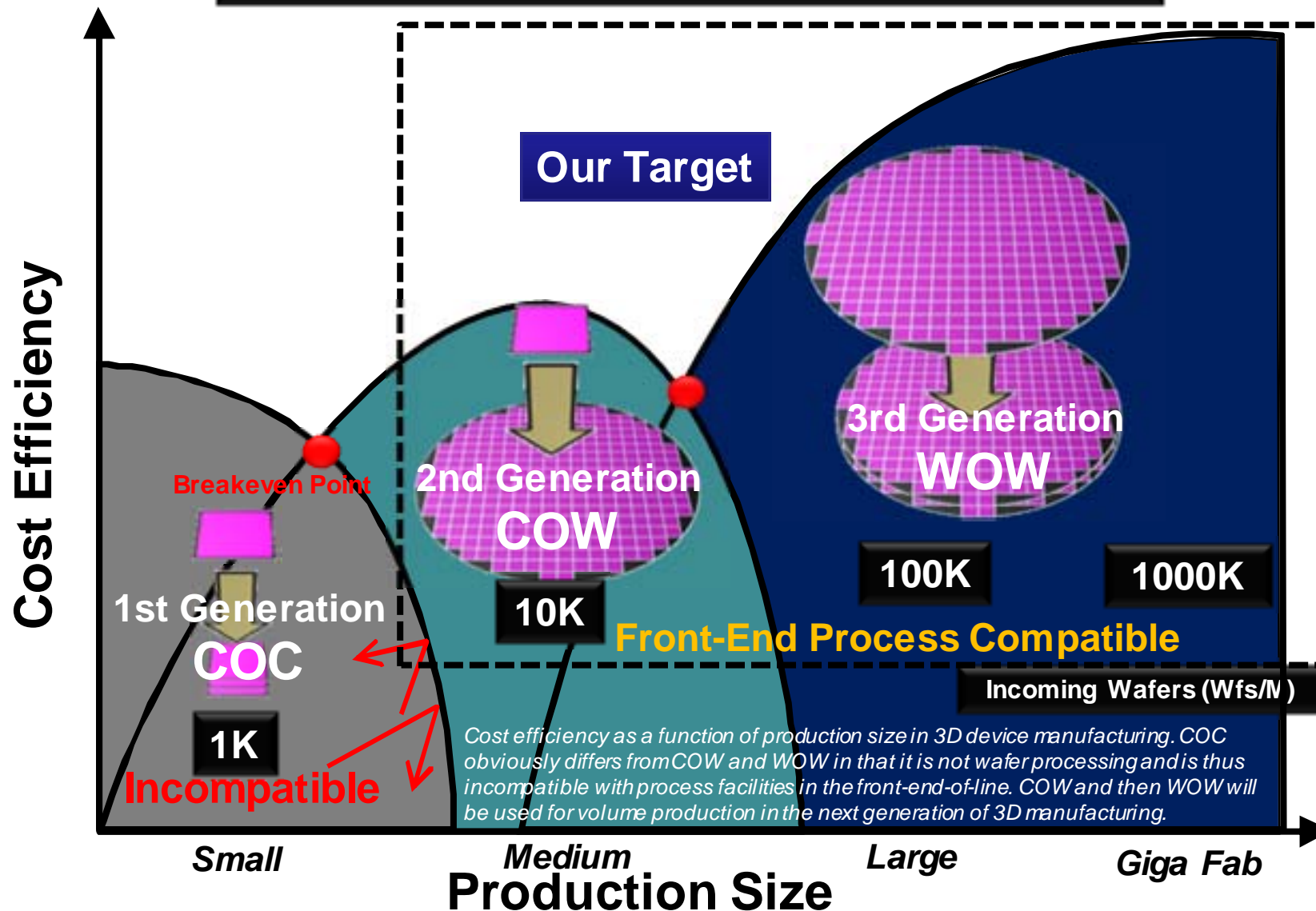
3DI Roadmap using WOW Technology



3D Market and Scaling for TSV Interconnects



3D Manufacturing Roadmap

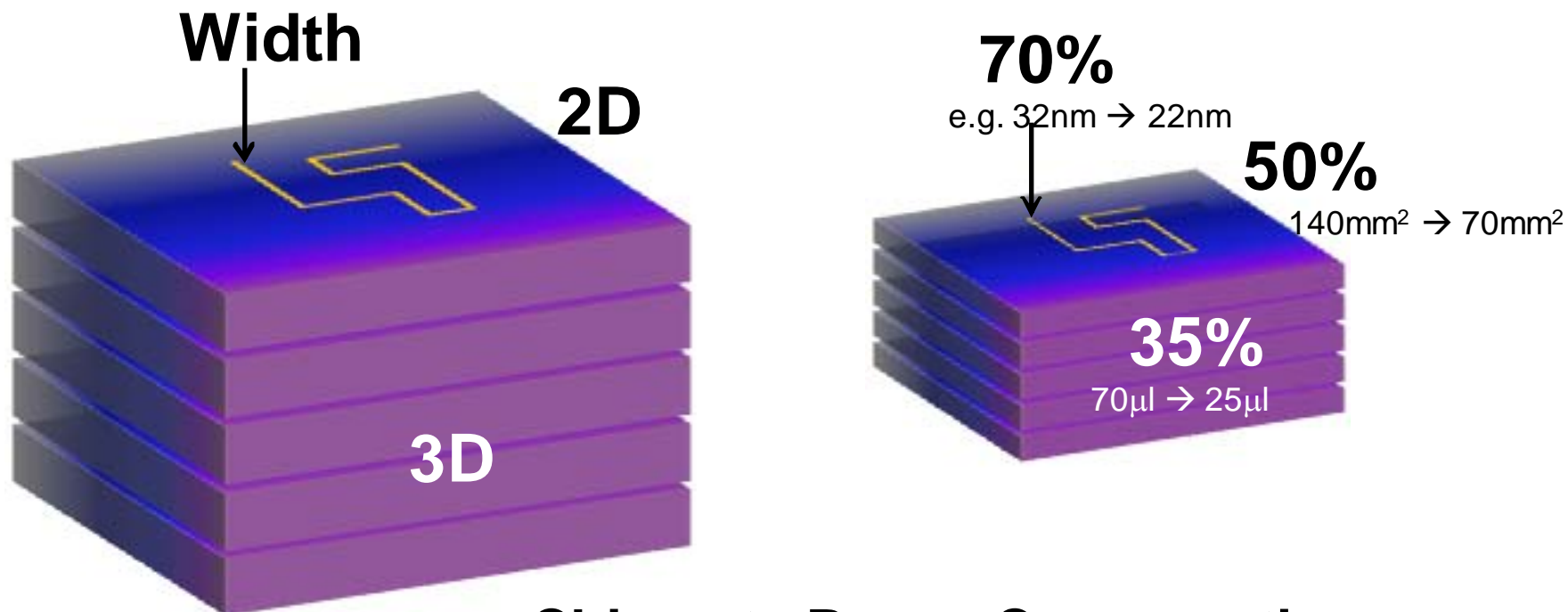


Coming 3D Era



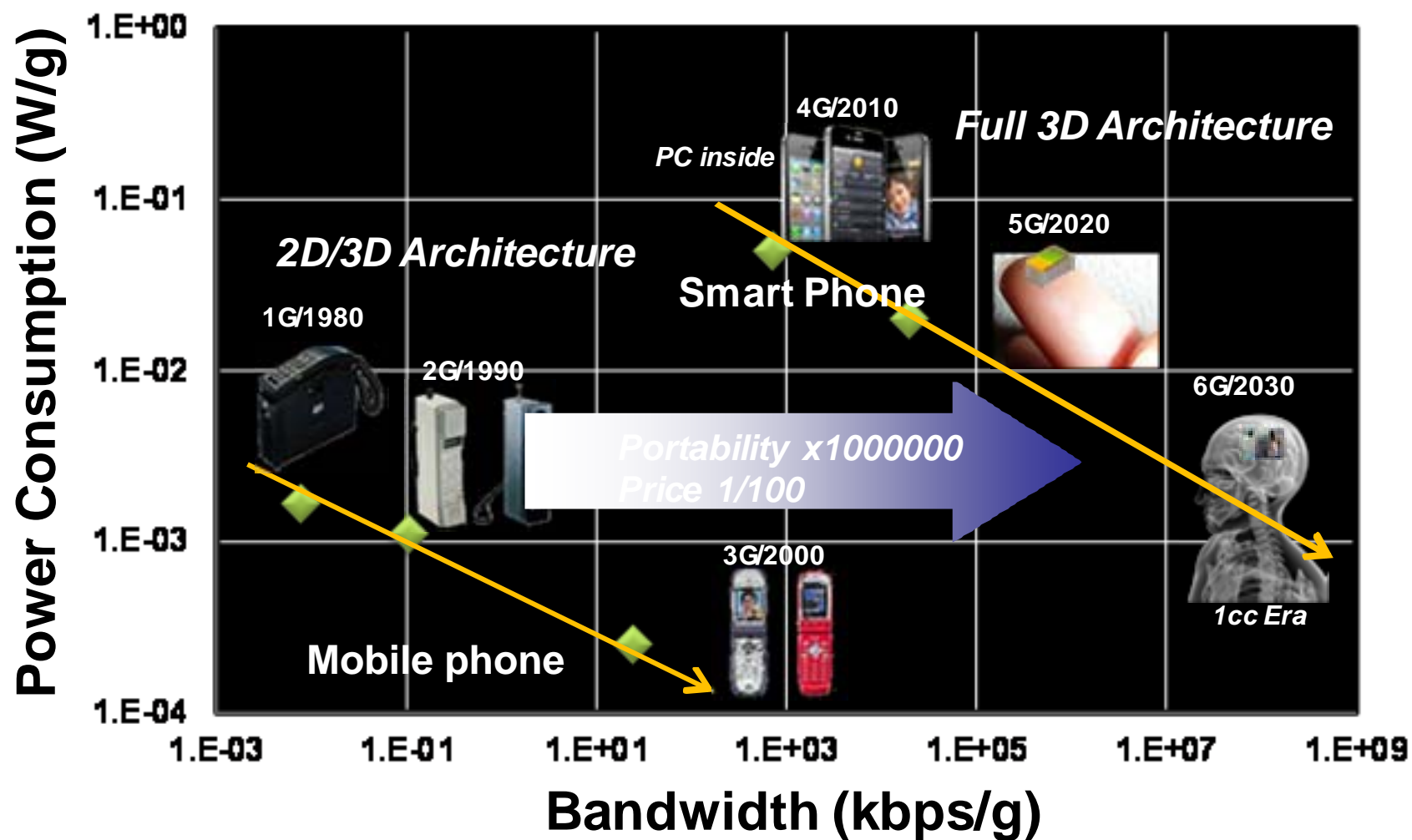
Scaling and Form Factor

Until now, huge 3D pictures have been proposed.
Today and Tomorrow, “3D as well as front-end processing” is **needed**.

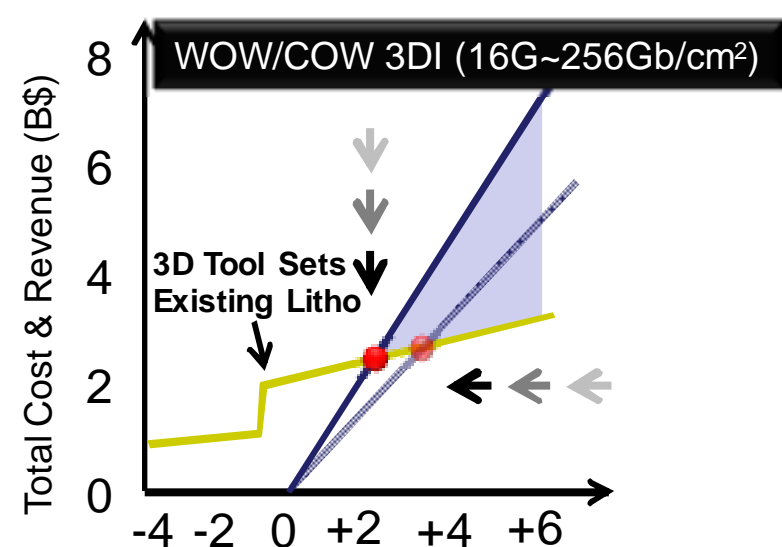
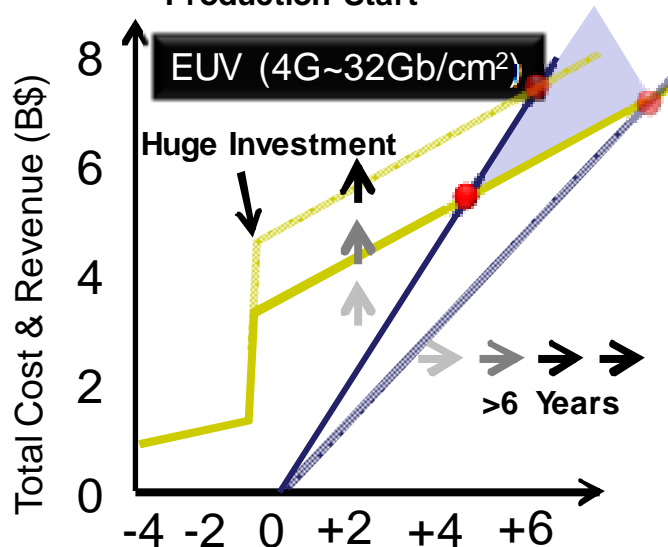
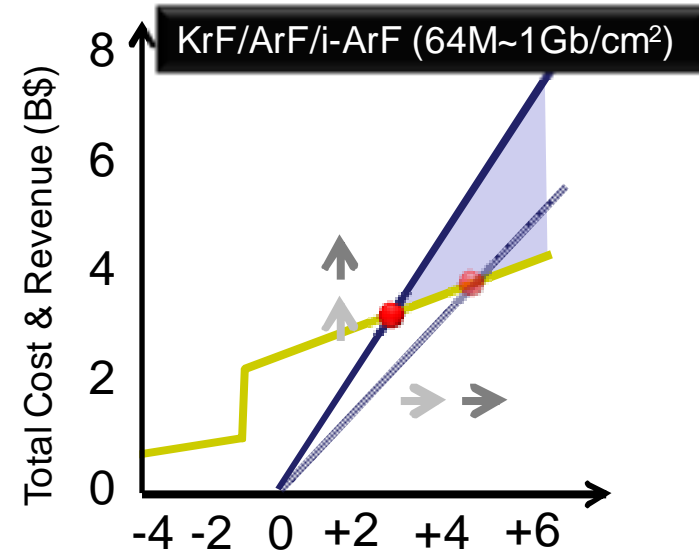
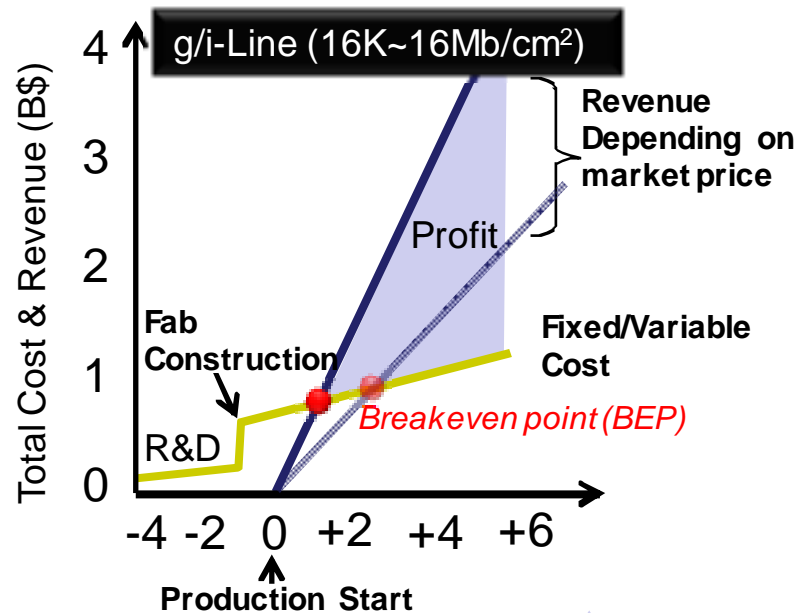


Chip-sets Power Consumption
2D/3D <1/10~1/100 (IO CLK 200MHz)

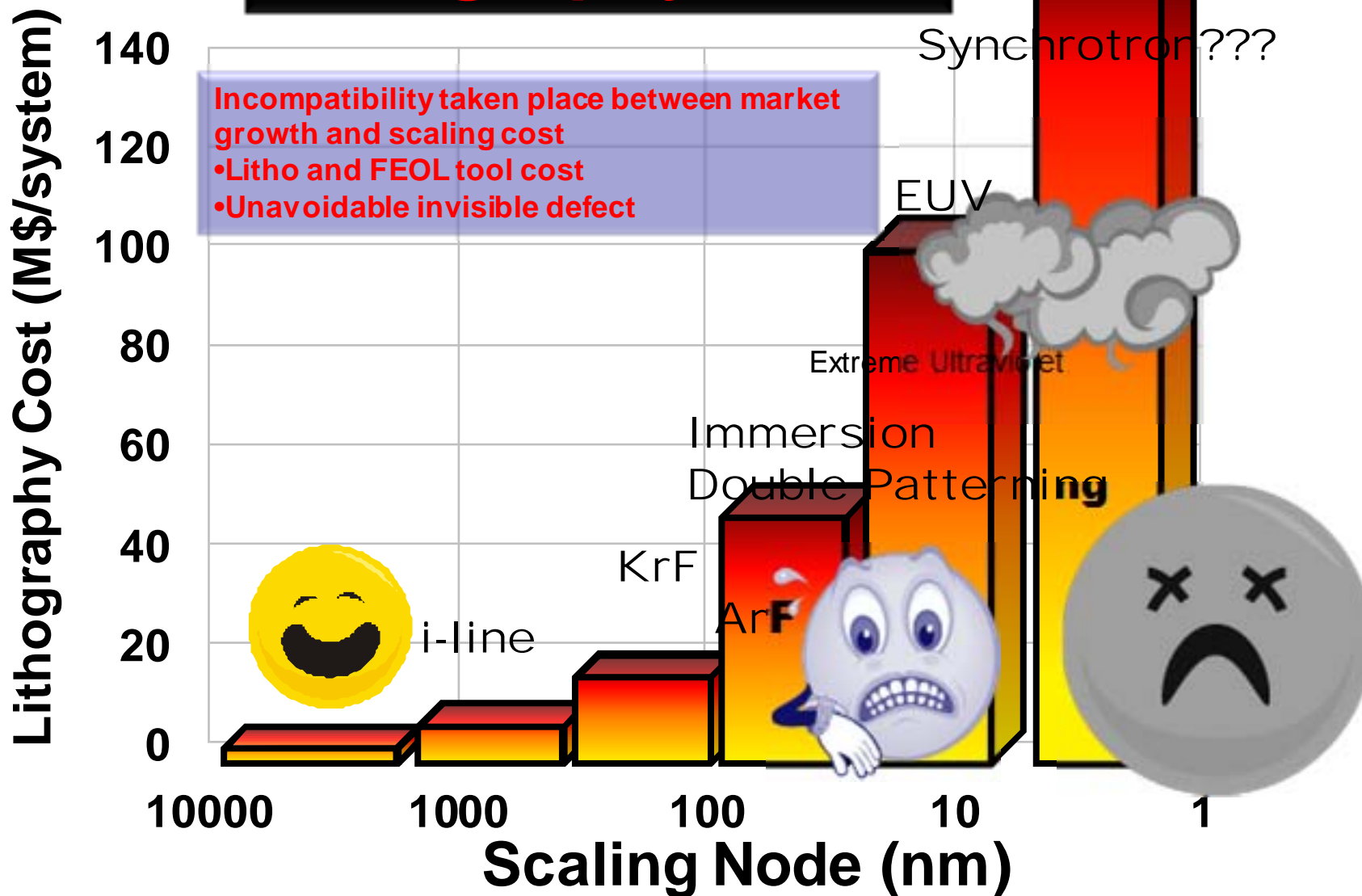
Trends of Mobiles



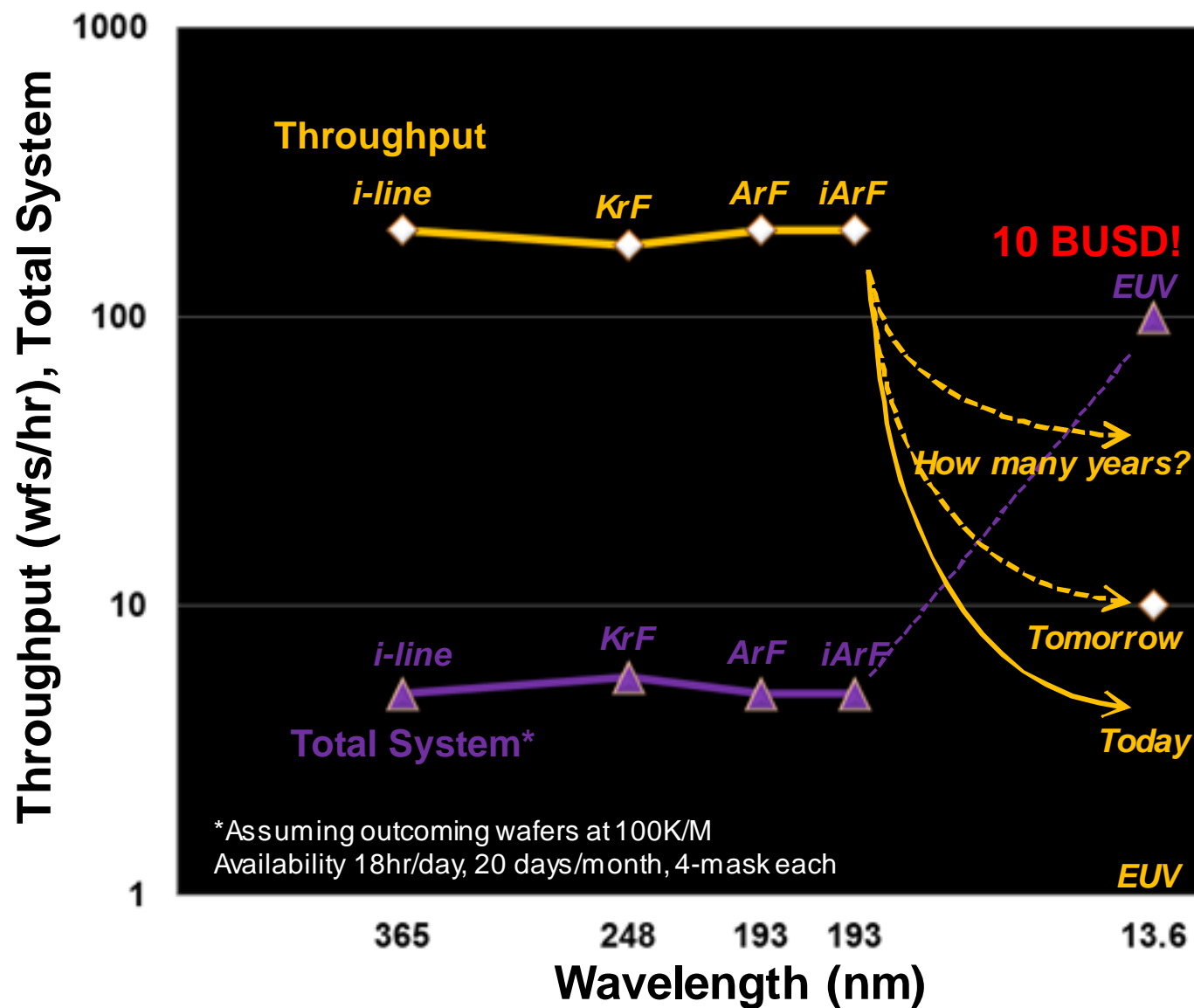
Profit Model in the Scaling



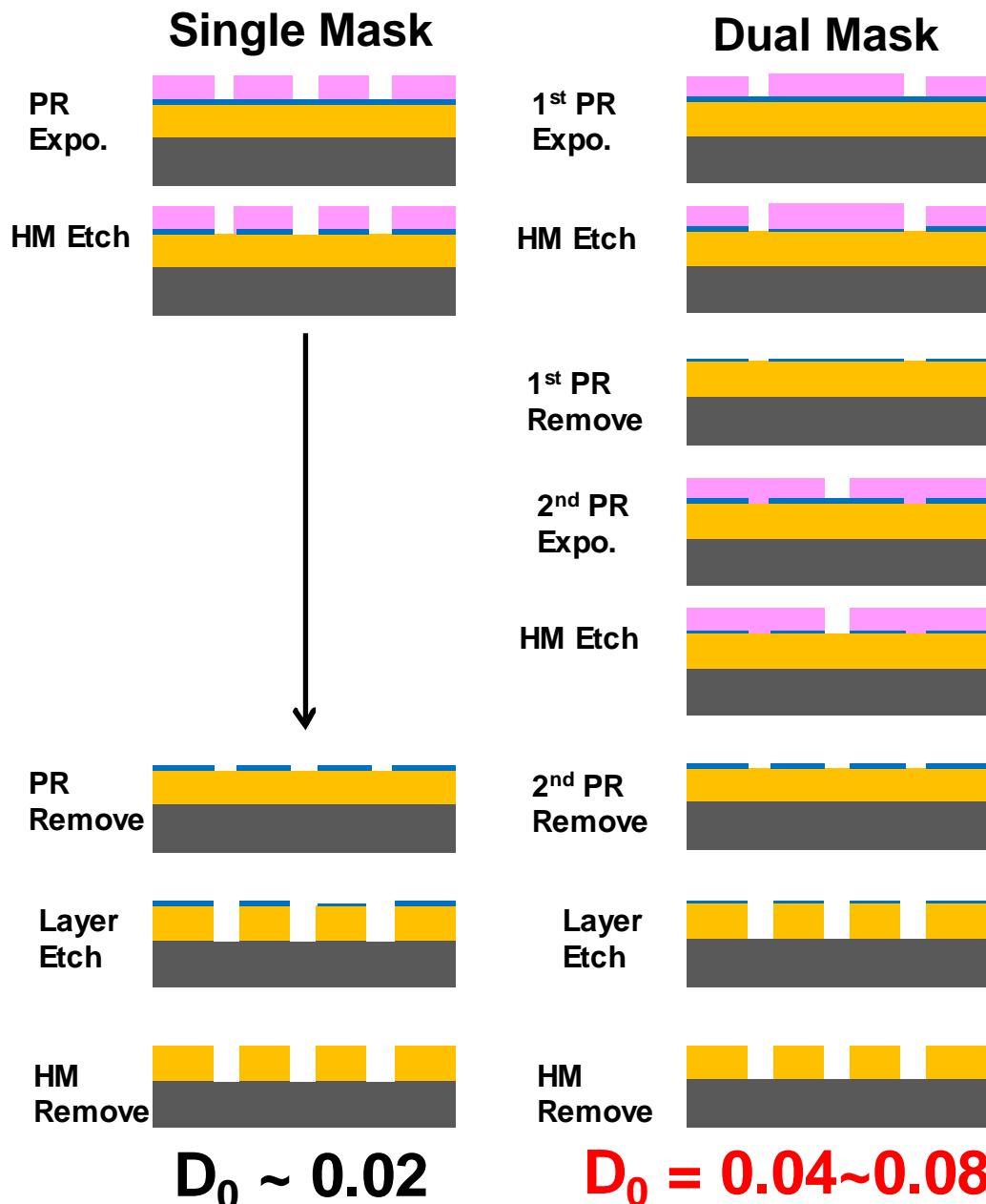
Lithography Cost!



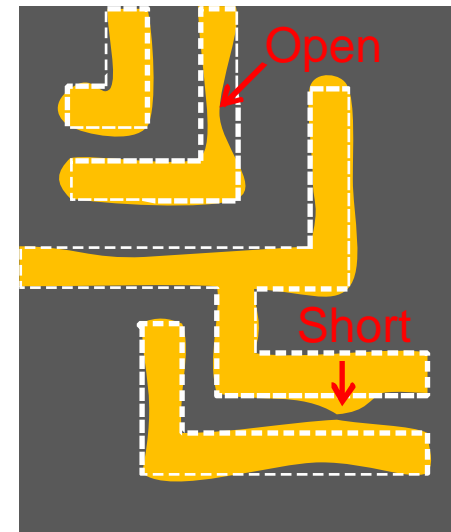
Throughput for Lithography



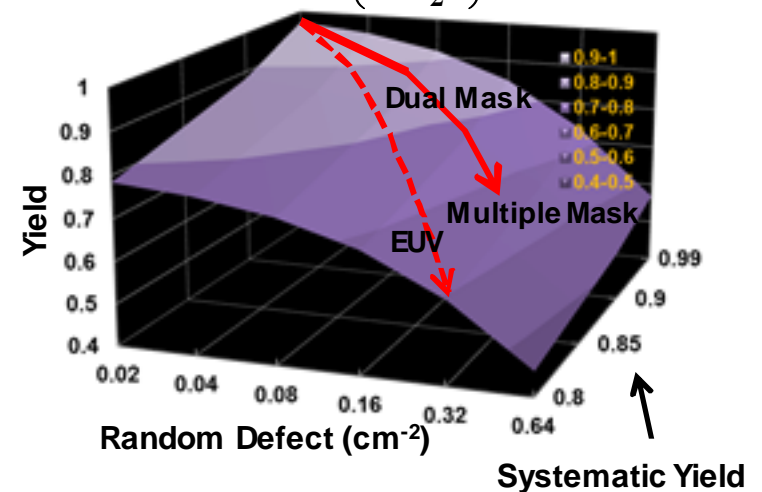
Yield Loss due to Defects in Critical Layers



Systematic Defects

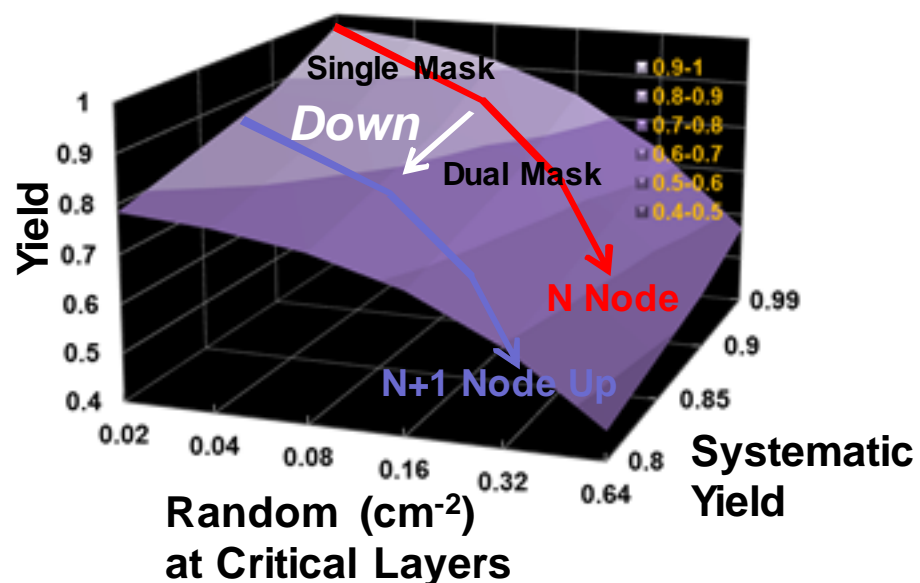


$$Y = Y_s \cdot \left(\frac{1}{1 + \frac{AD_0}{2}} \right)^2$$



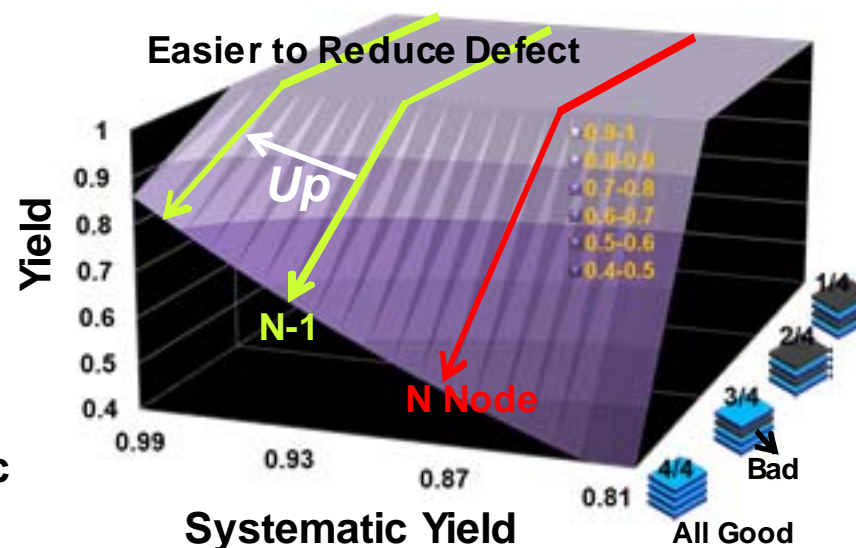
Comparison of Yield for Large Integration

Scaling (Dual-Mask Patterning)



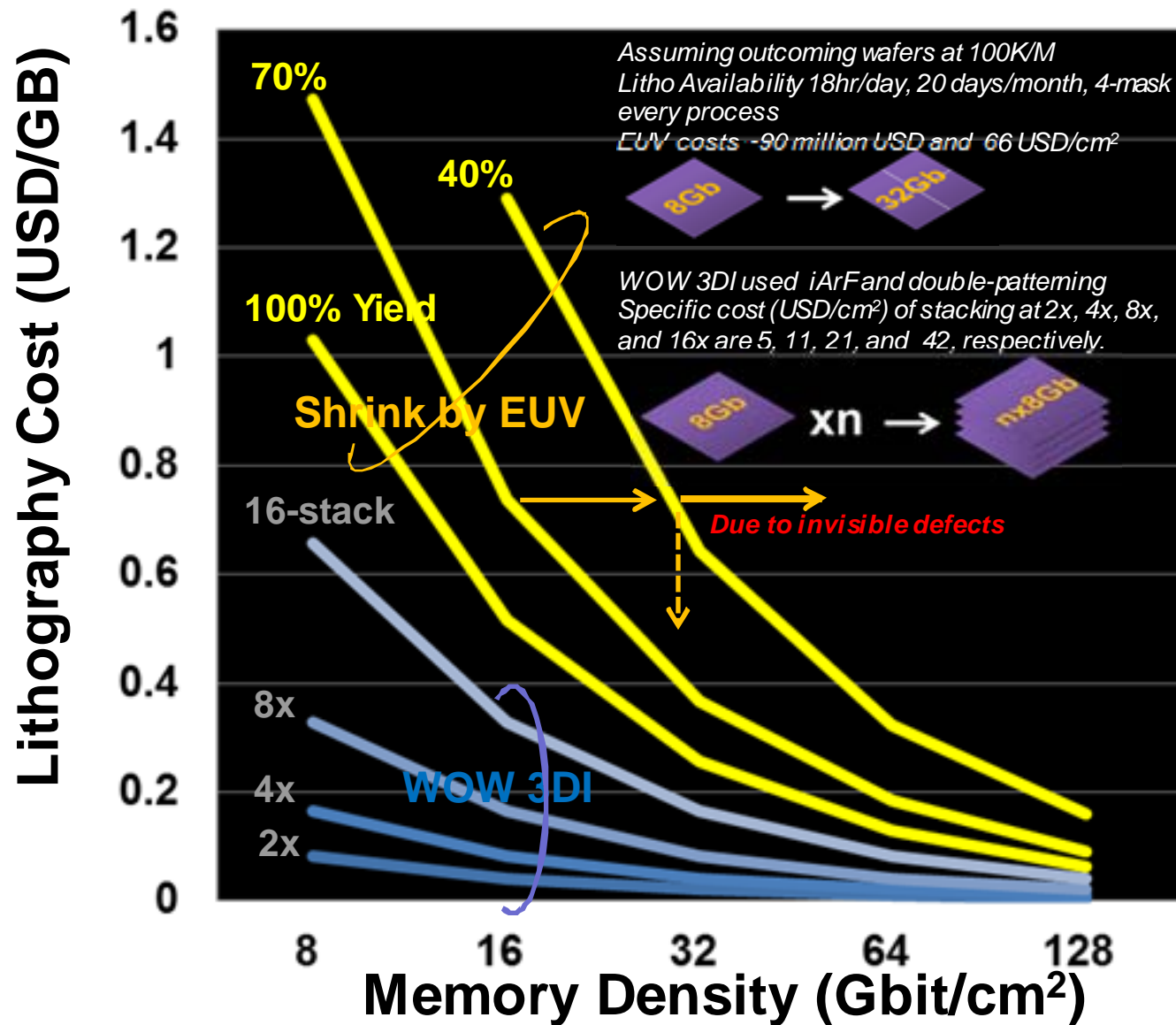
Assumptions:
 CD < 22nm
 Dual mask and dual exposure
 Hard mask and single etching
 Die size (A) = 1.0 cm²

3D Wafer Stack (4-stack)



Assumptions:
 CD = 32~45 nm
 Four wafer stack using multi bumpless TSV
 No contact failure on TSVs
 Random Defects (D_0) = 0.1 cm⁻²
 Die size (A) = 1.148 cm²

Lithography Cost as a Function of Memory Density



Technology Driver in Semiconductor

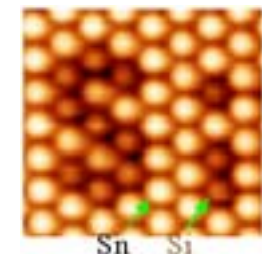
2D Wafer Integration Technology



~45nm by ArF



~22nm by Immersion



Y. Sugimoto et al.,
 Science, Vol.322 (2008)
 pp.413-417

Hopefully...EUV

~1nm

3D Wafer Integration Technology

3DI WOW Technology

10μm Ultra-Thinning



300mm w/ Existing nodes

Various Applications

DRAM/DRAM
 Flash/Flash
 DRAM/MPU
 MPU/MEMS
 MEMS/MEMS

Large integration w/o limitation



Multi Wafer Stack

4G/2-stack
 8G/4-stack
 16G/8-stack
 ...
 1T/256-stack
 2T/1k-stack

Twitting somebody on 450mm Enlargement

2025年かな

ネタが増えた

ヤルノヨ!

本当かな～

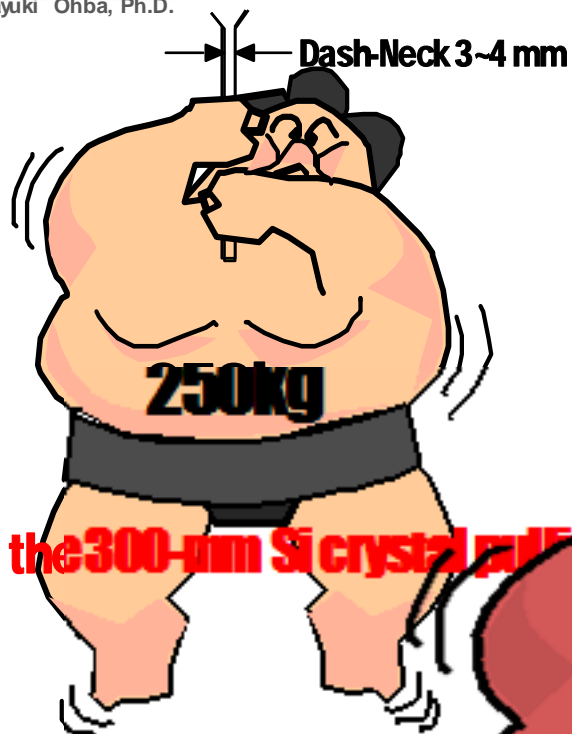
450mm Wafer



300mm Wafer



Experience on Wafer enlargement
6inch → 8inch Two Year Delayed
8inch → 12inch Five Year Delayed
12inch → 450mm, more than 10 Years?



300mm vs 450mm

x8000!

What is the 300mm Si crystal pulling?

There was enough economic
It was Win & Win relation among



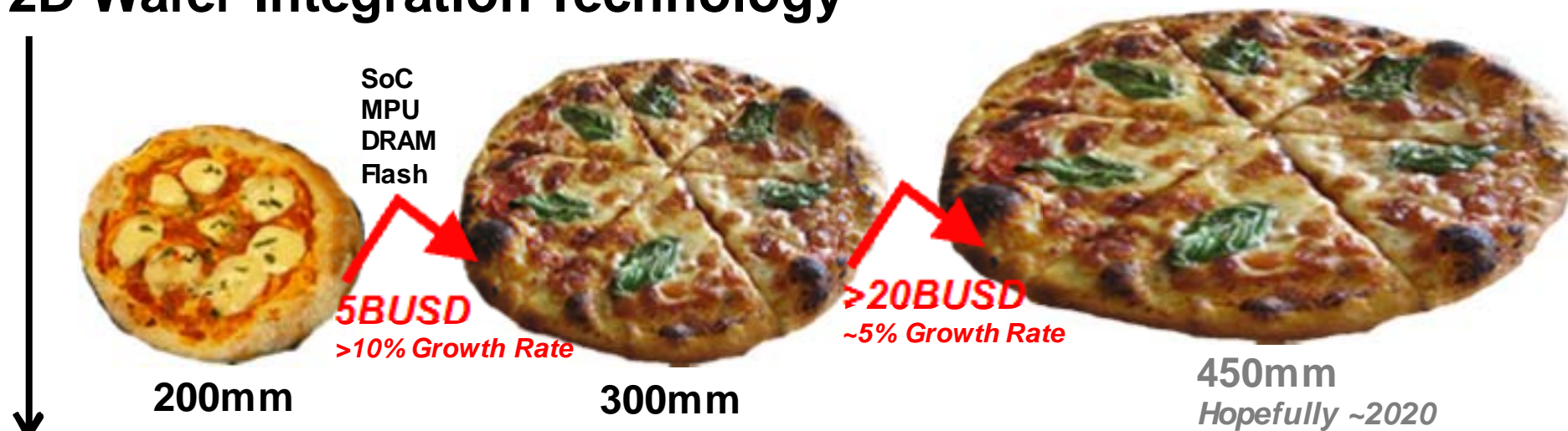
What is the 300mm Si crystal pulling?

450mm

Situation has been changed.

Technology Driver in Semiconductor

2D Wafer Integration Technology



3D Wafer Integration Technology

Large Si Surface more than that of 450mm

3DI WOW Technology

10μm Ultra-Thinning



200mm and 300mm

Various Applications

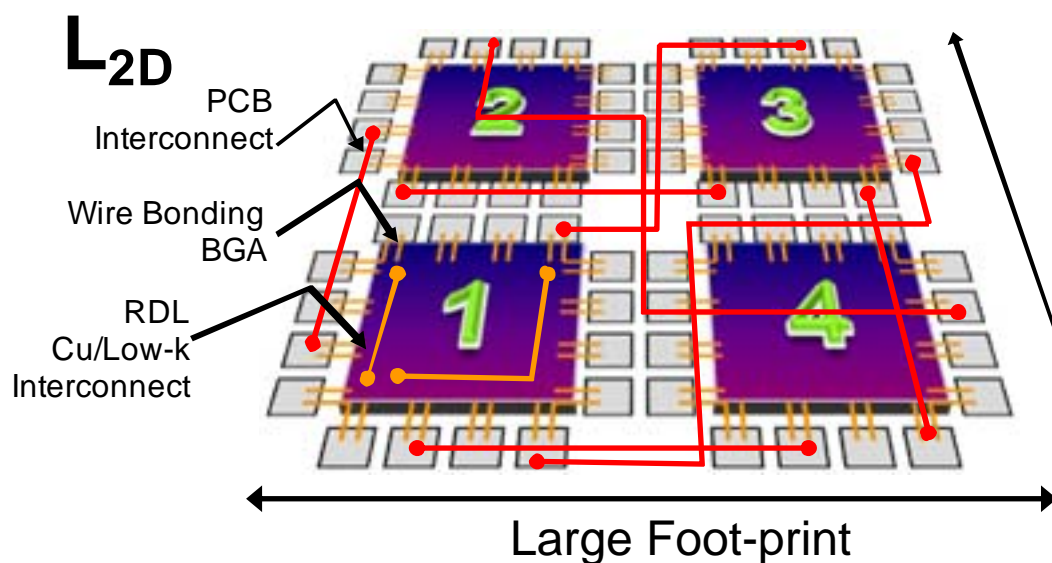
DRAM/DRAM
 Flash/Flash
 DRAM/MPU
 MPU/MEMS
 MEMS/MEMS



Multi Wafer Stack

2-stack
 4-stack
 8-stack
 ...
 256-stack
 1k-stack

Advantages of 3D Integration



2D Chip Set

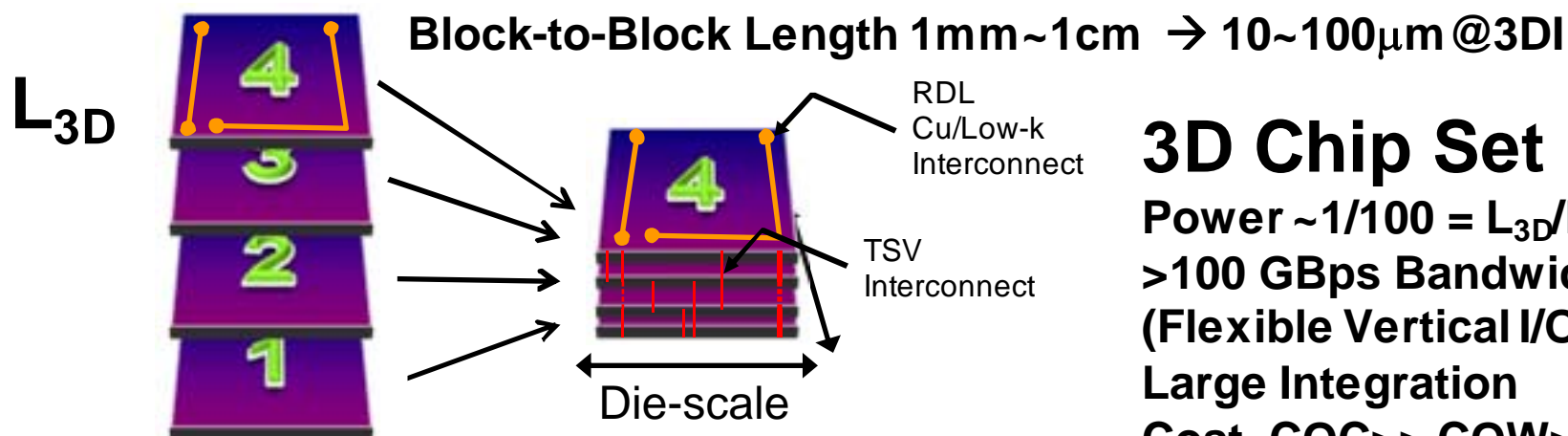
$$Power = N(f \cdot C \cdot V_{DD}^2 + I_{off} \cdot V_{DD})$$

$$P_{Tr} \approx \ln W / MHz / Tr$$

$$\uparrow \text{Bandwidth} \sim S / L^2 \downarrow$$

$$\downarrow \text{RC Delay} \sim L^2 \downarrow S$$

$$\downarrow \text{Wiring Capacitance} \sim L \downarrow H / d$$



3D Chip Set

$$Power \sim 1/100 = L_{3D} / L_{2D}$$

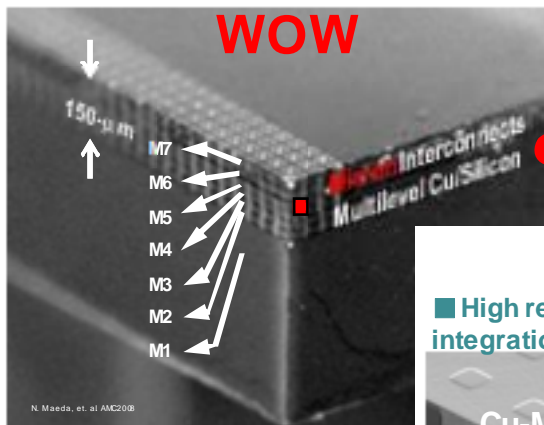
>100 GBps Bandwidth
(Flexible Vertical I/O)

Large Integration

Cost COC >> COW > WOW

AMC2008

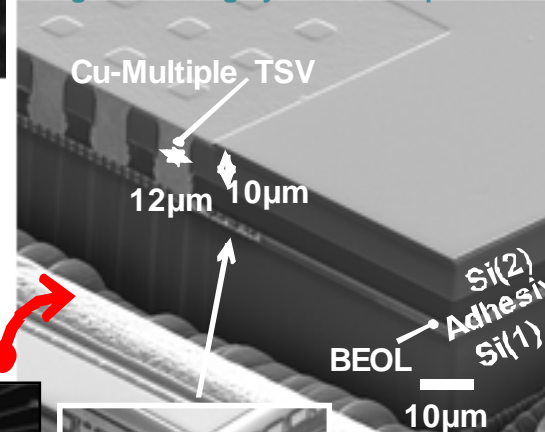
■ Wafer level Ultra thin 7 stacked TSV's



Bumpless Interconnects

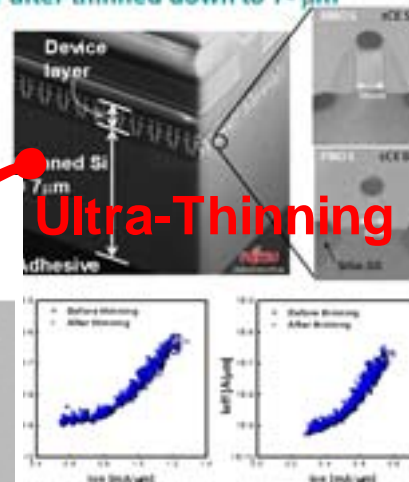
IITC2010

■ High reliability multiple TSV integration using by LT-PECVD process



IEDM2009

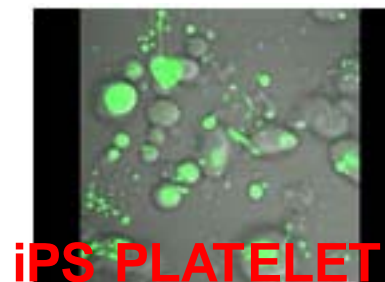
■ No degradation of 45nm-node strained Tr after thinned down to 7-μm



Ultra-Thinning

VLSI2012

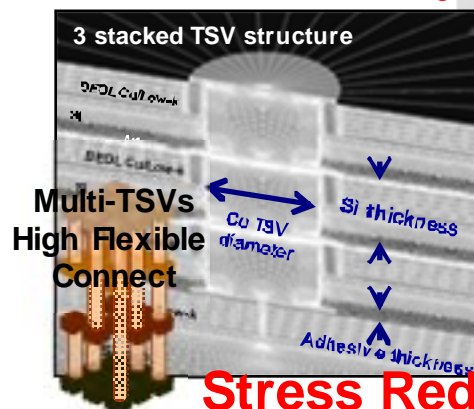
COW



TSV's process

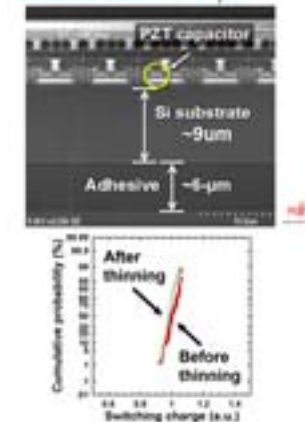
IITC2009, MRS2009

■ Design for lower thermal stress



VLSI2010

■ No degradation of FRAM after thinned down to 9-μm

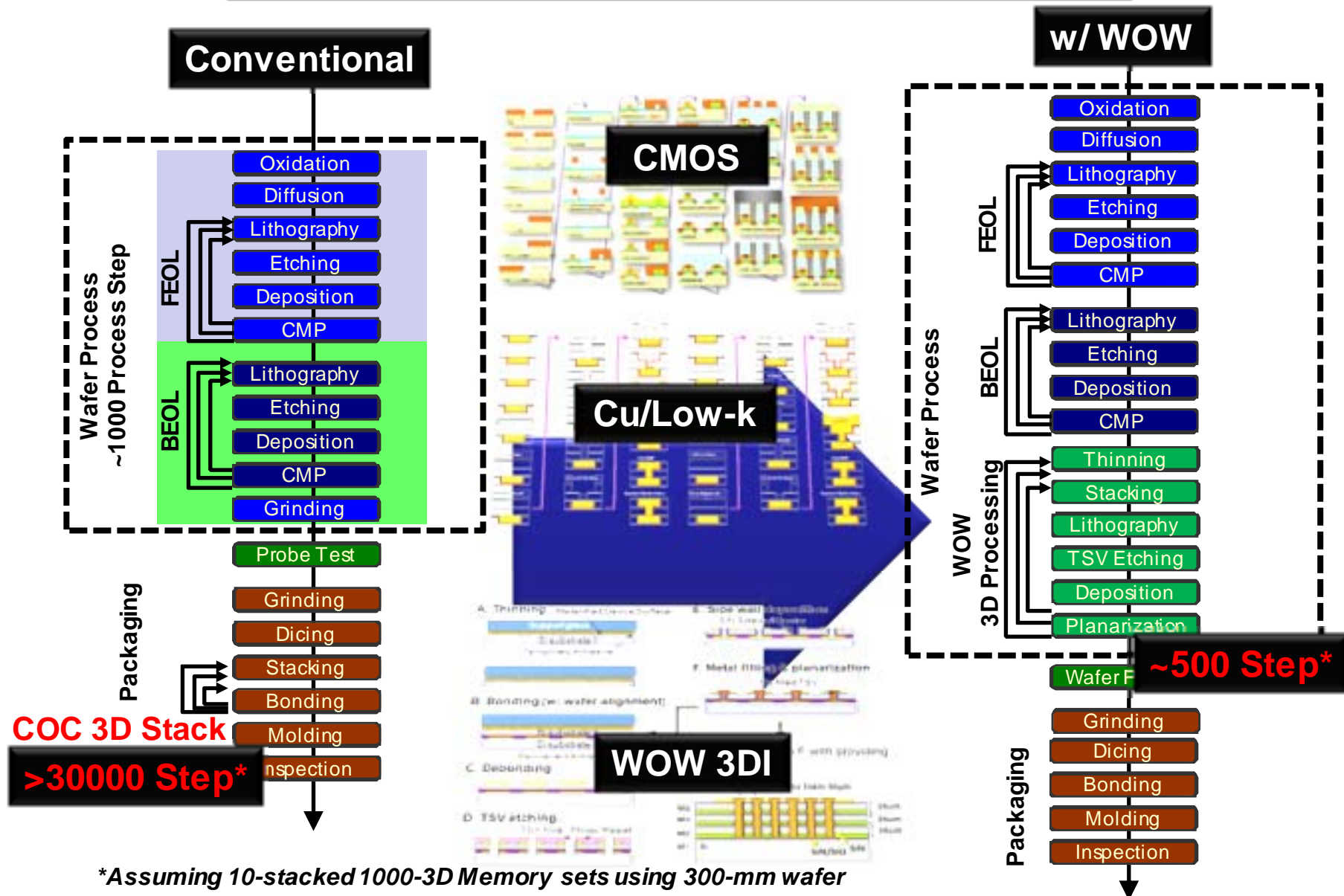


VLSI2011

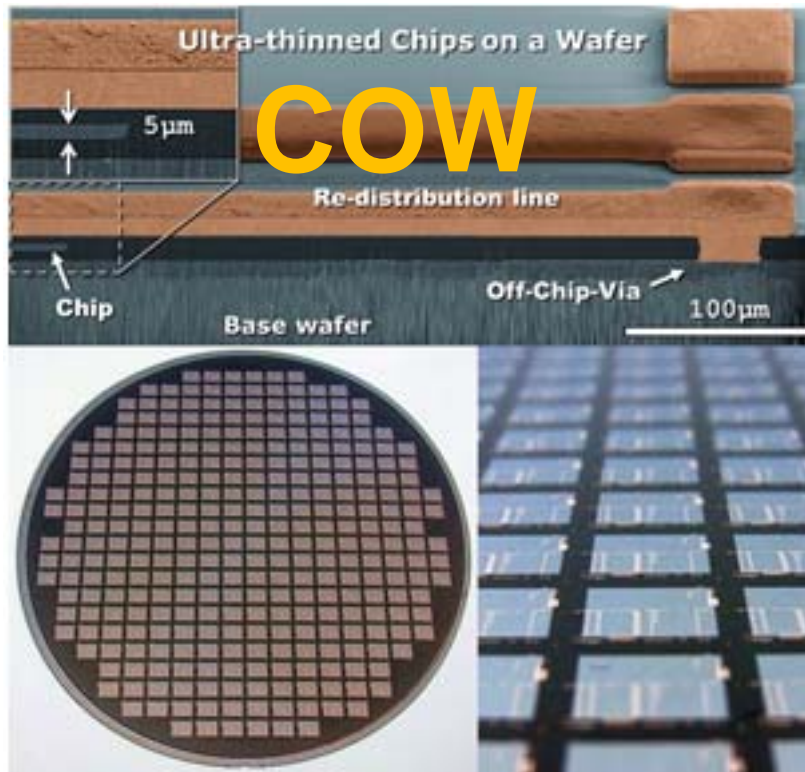
■ Micro channel closed loop system



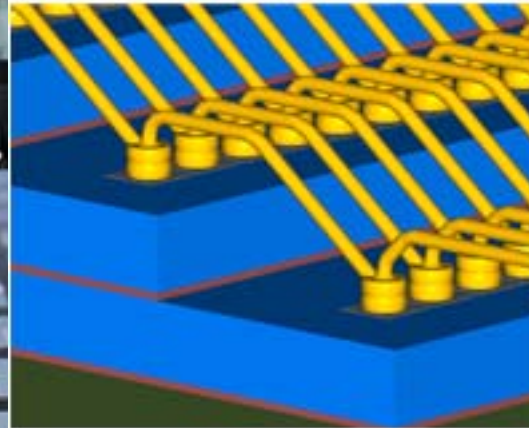
Next Manufacturing Scheme



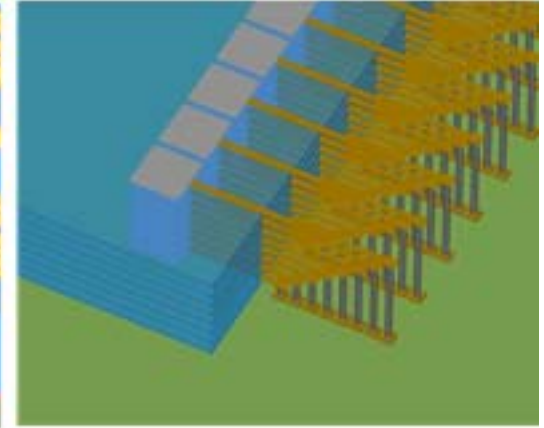
Bumpless Interconnects for WOW/COW



Conventional WB



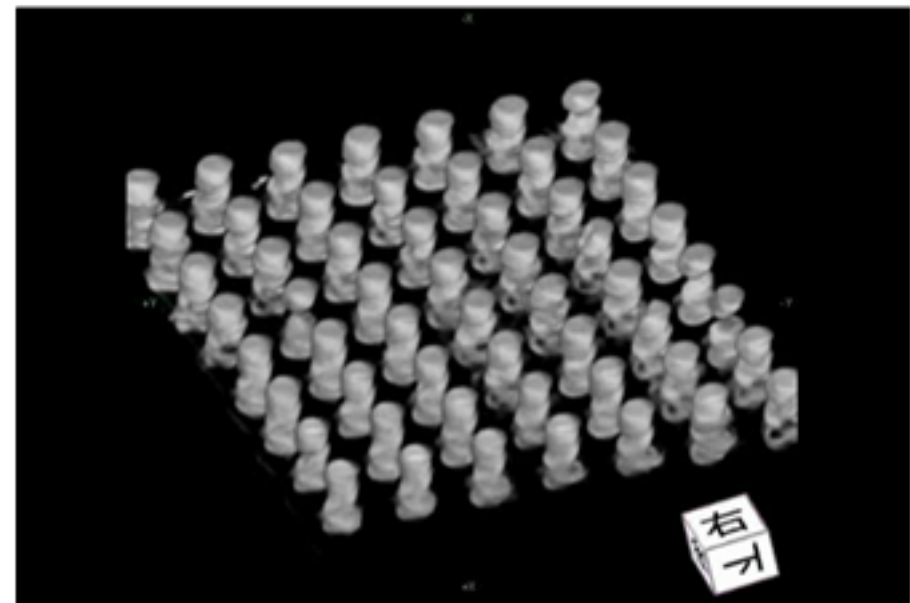
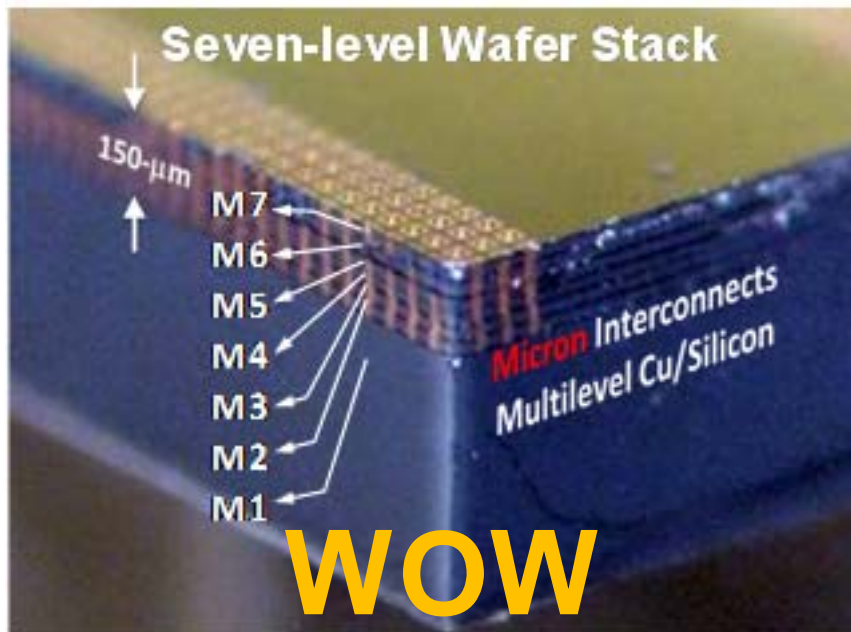
COW off-chip Vias



Thinning-First and then Vertical Interconnection Processes

Bumpless Interconnects for WOW/COW

Multi-stack Wafers

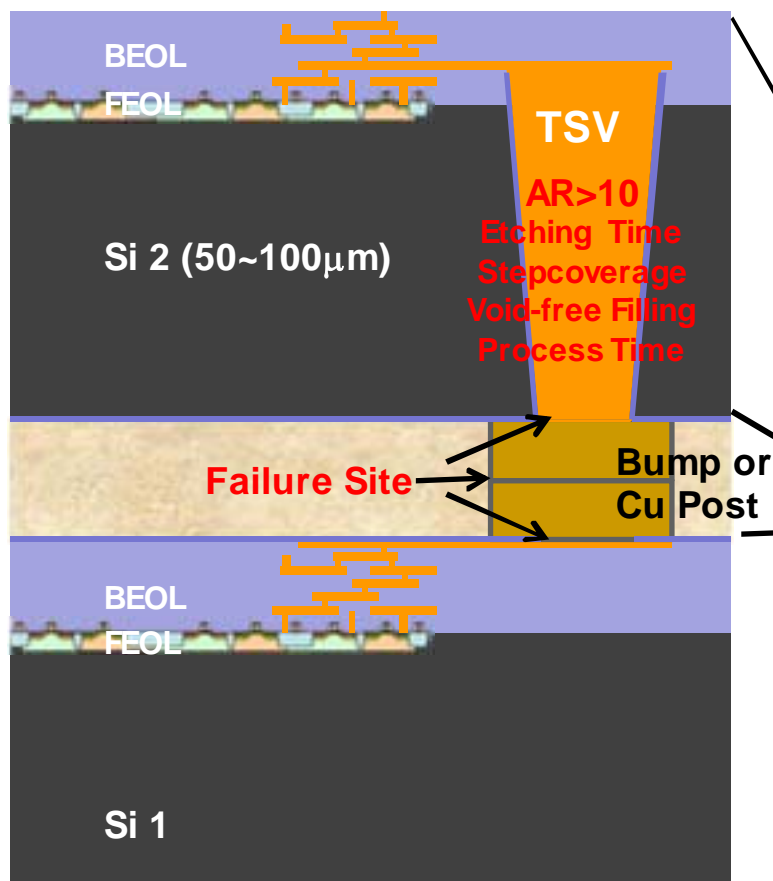


Thinning-First and then Vertical Interconnection Processes

A Comparison of TSV Interconnects

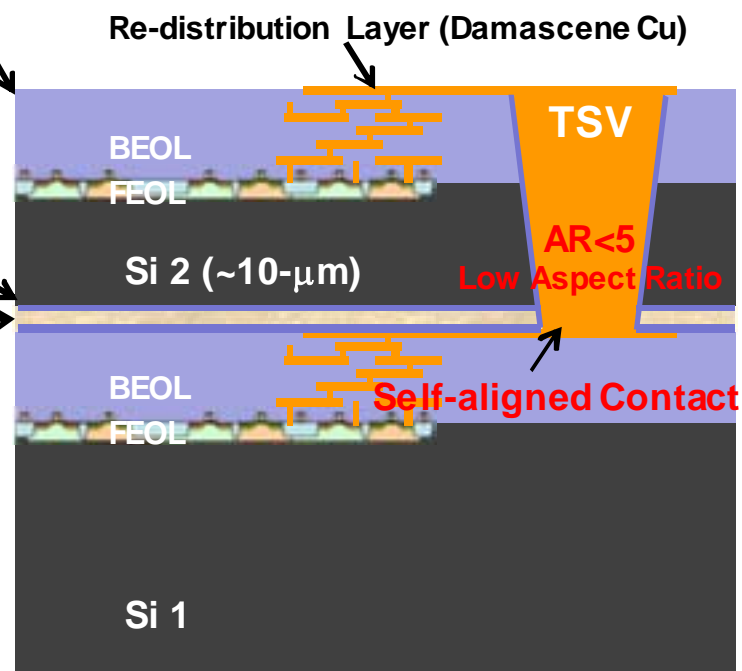
Conventional with Bump

Via-last/middle, Thinning-last



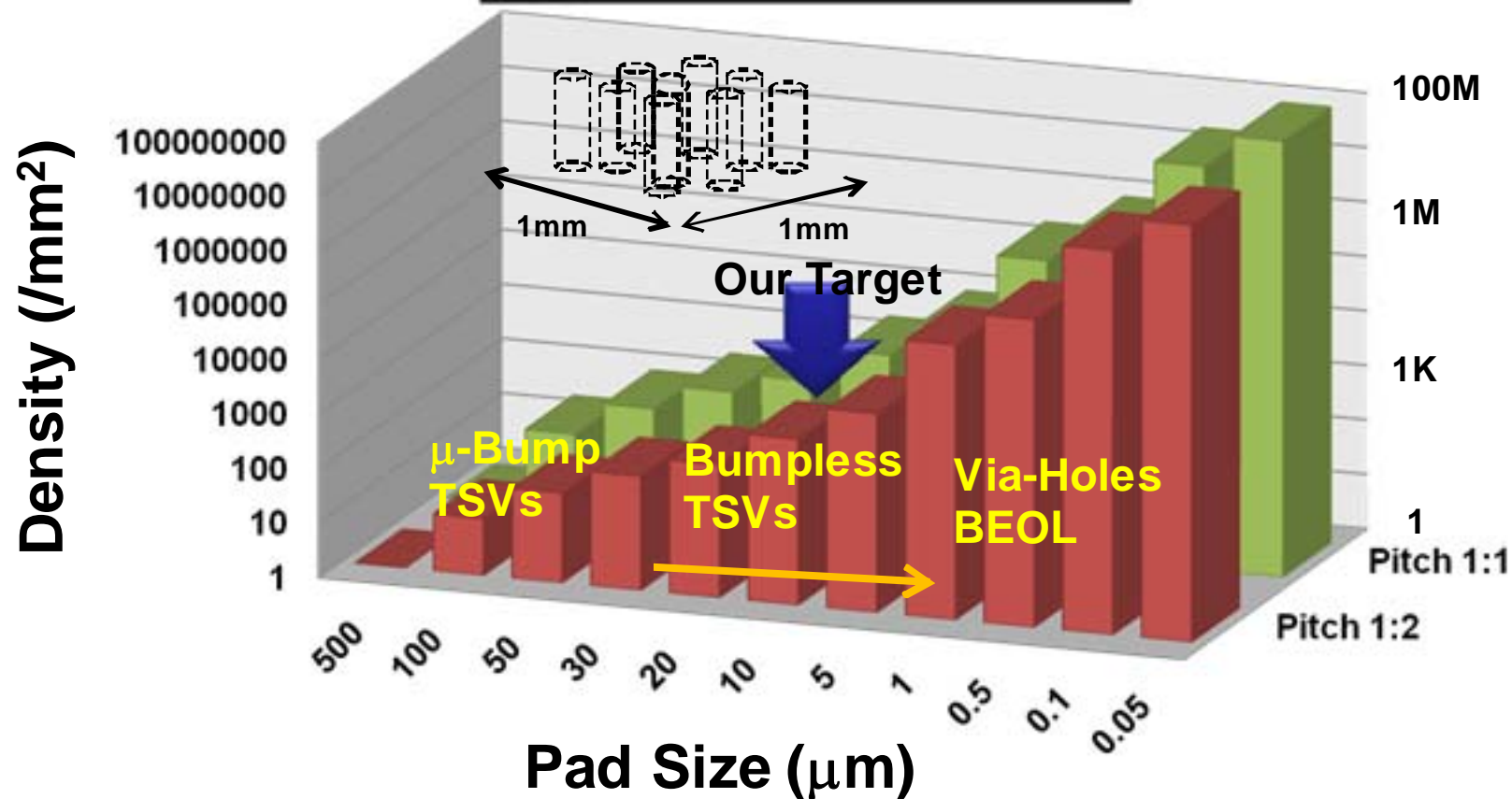
Bumpless Damascene TSV

Thinning-first, Via-last

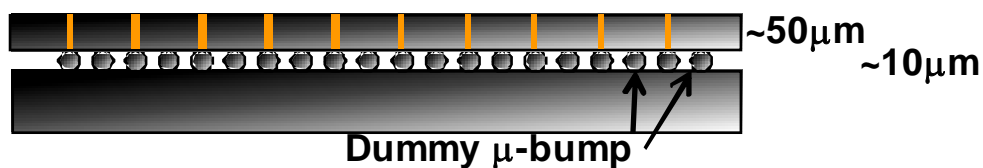


Comparison of conventional TSV using bump electrode (left) and bumpless TSV (right) for WOW and COW technologies. The aspect ratio decreases with thinning of wafer and becomes less than 5 at the total thickness and diameter of TSV of 25 μm and 5 μm, respectively.

TSV/Via Density



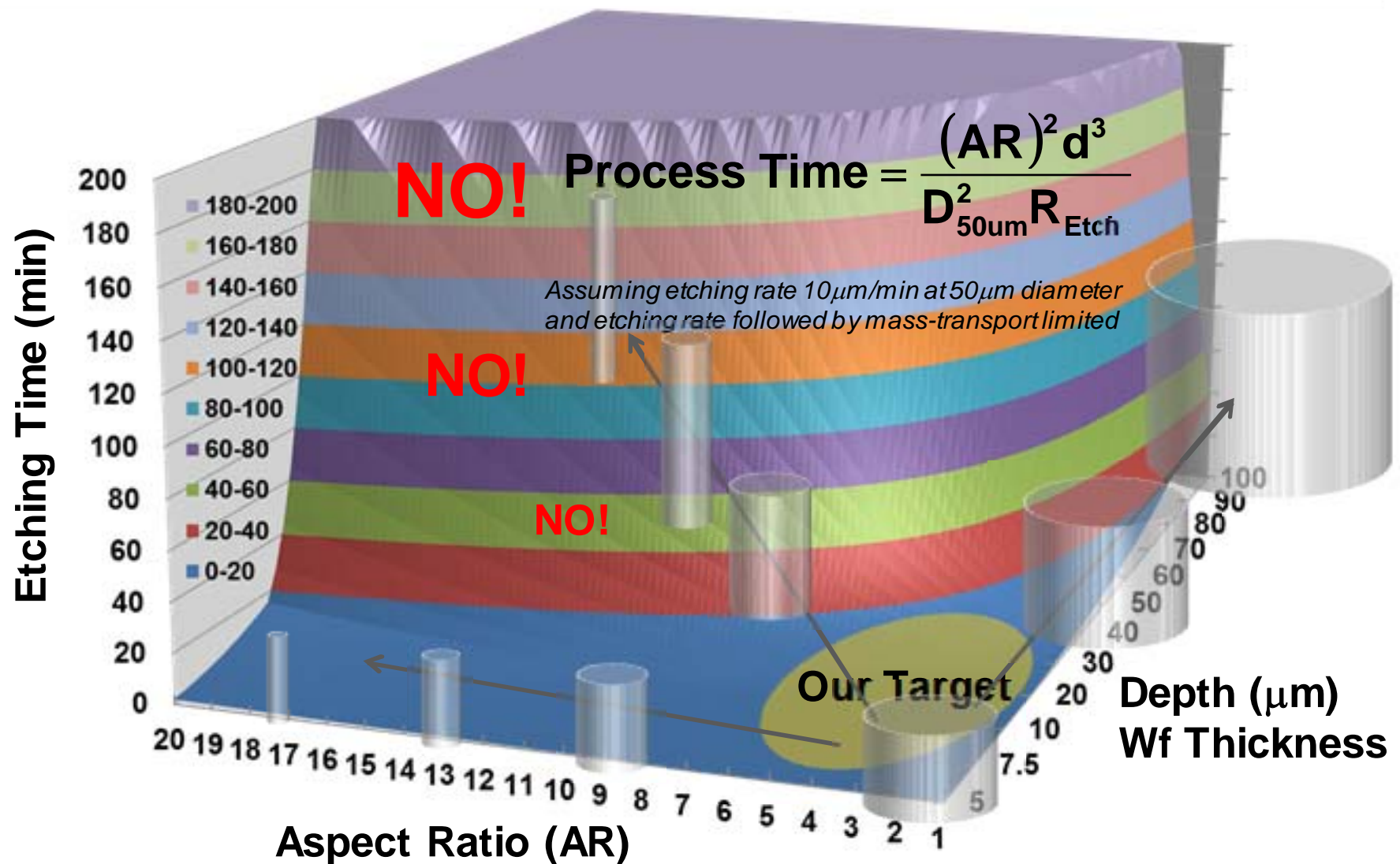
Conventional Bump and TDSVs



Bumpless TDSVs



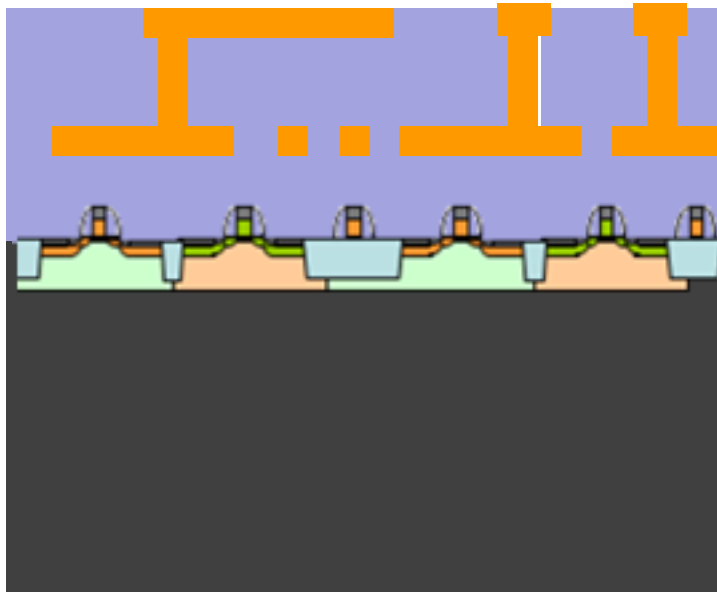
Bumpless and Ultra Thinning Enables Higher Throughput



Front-end Compatible Process

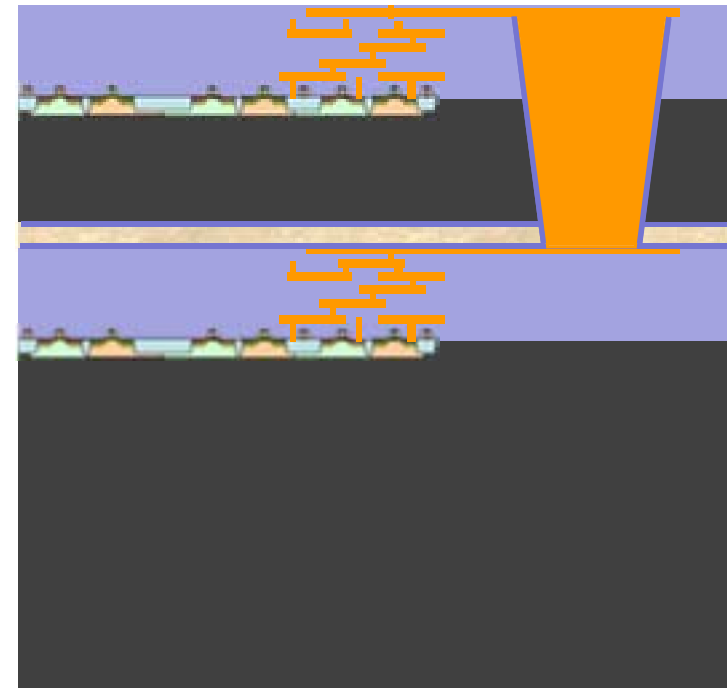
Cu/Low-k Interconnects

- ✓ Dielectrics Deposition
- ✓ Dual-Damascene Etching
- ✓ Cu Plug and Metallization



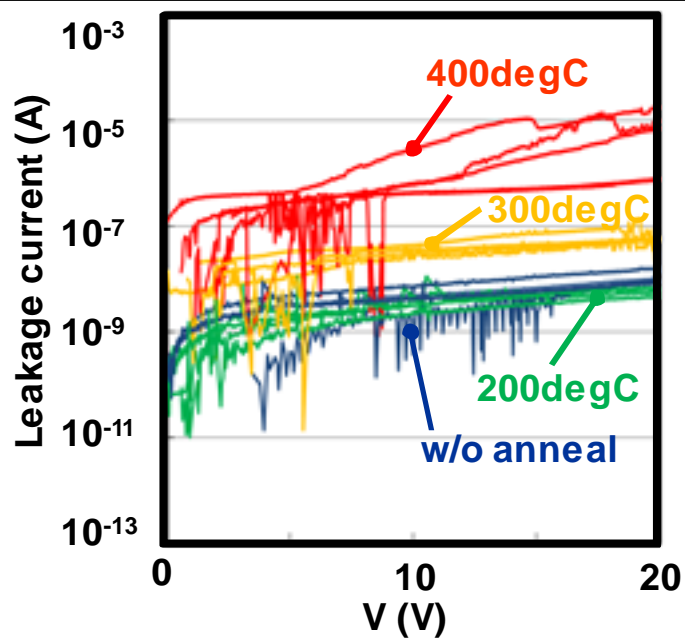
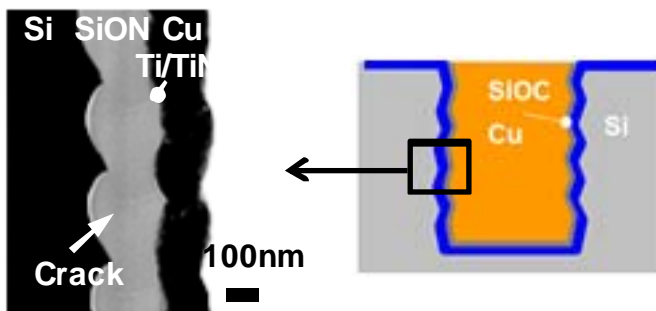
Cu/Si Interconnects

- ✓ Thinned Wafer Bonding
- ✓ Dual-Damascene TSV Etching
- ✓ Cu Plug and Metallization

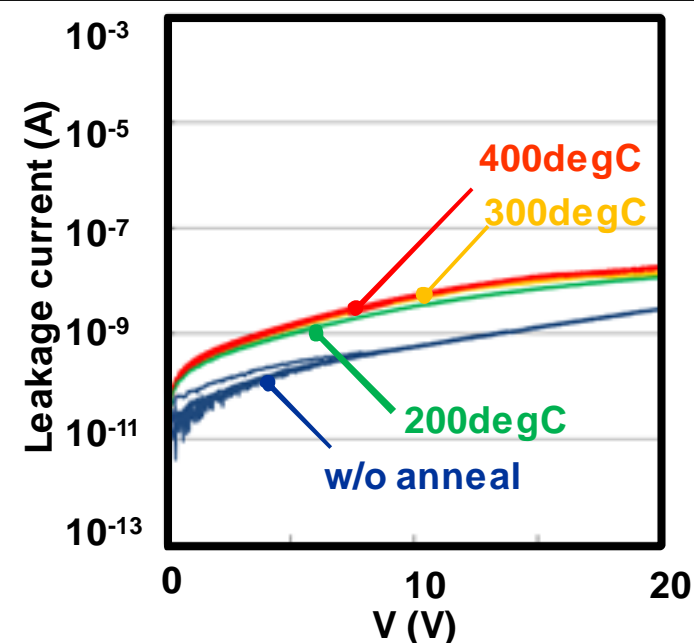
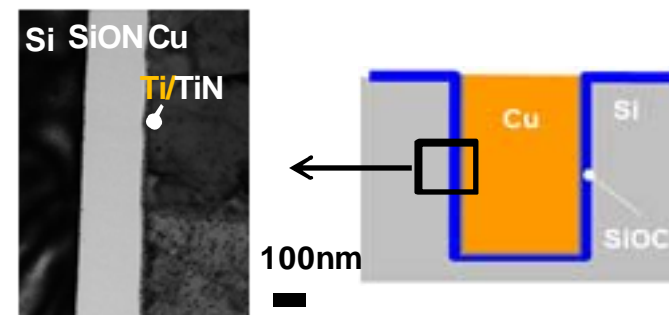


Comparison of Leakage Current

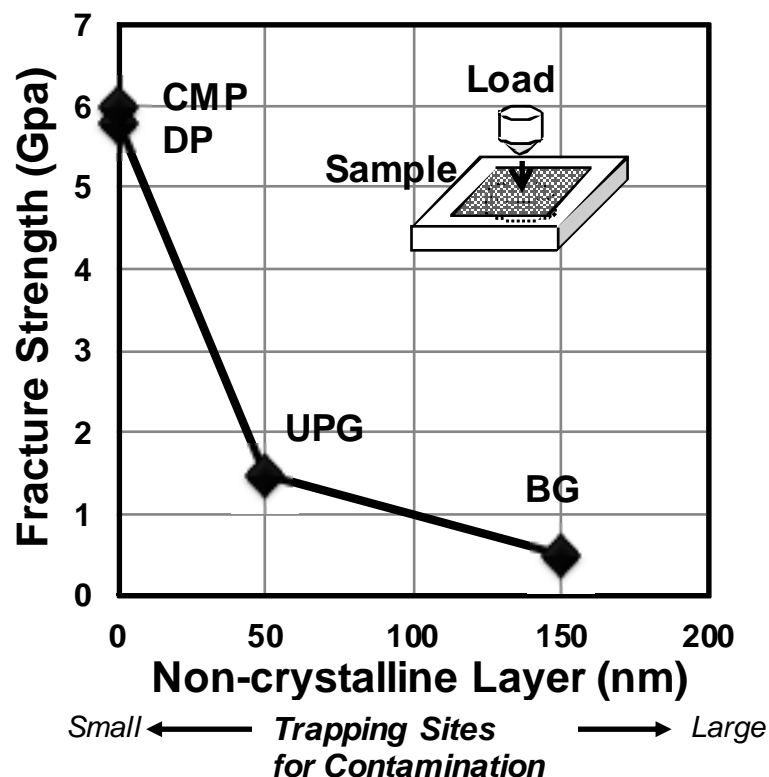
Bosch etching



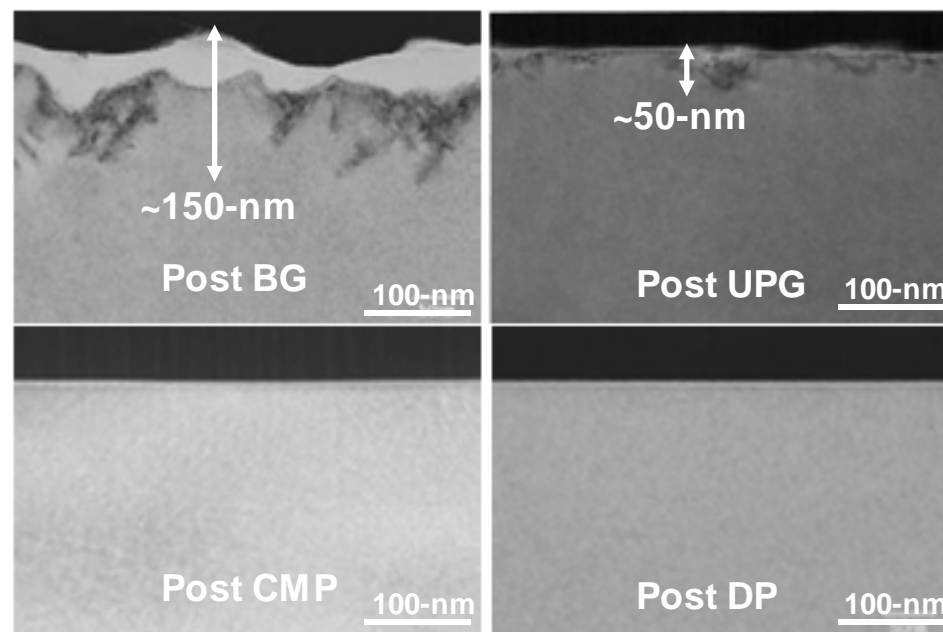
Direct etching



Thinning Module Cont'd

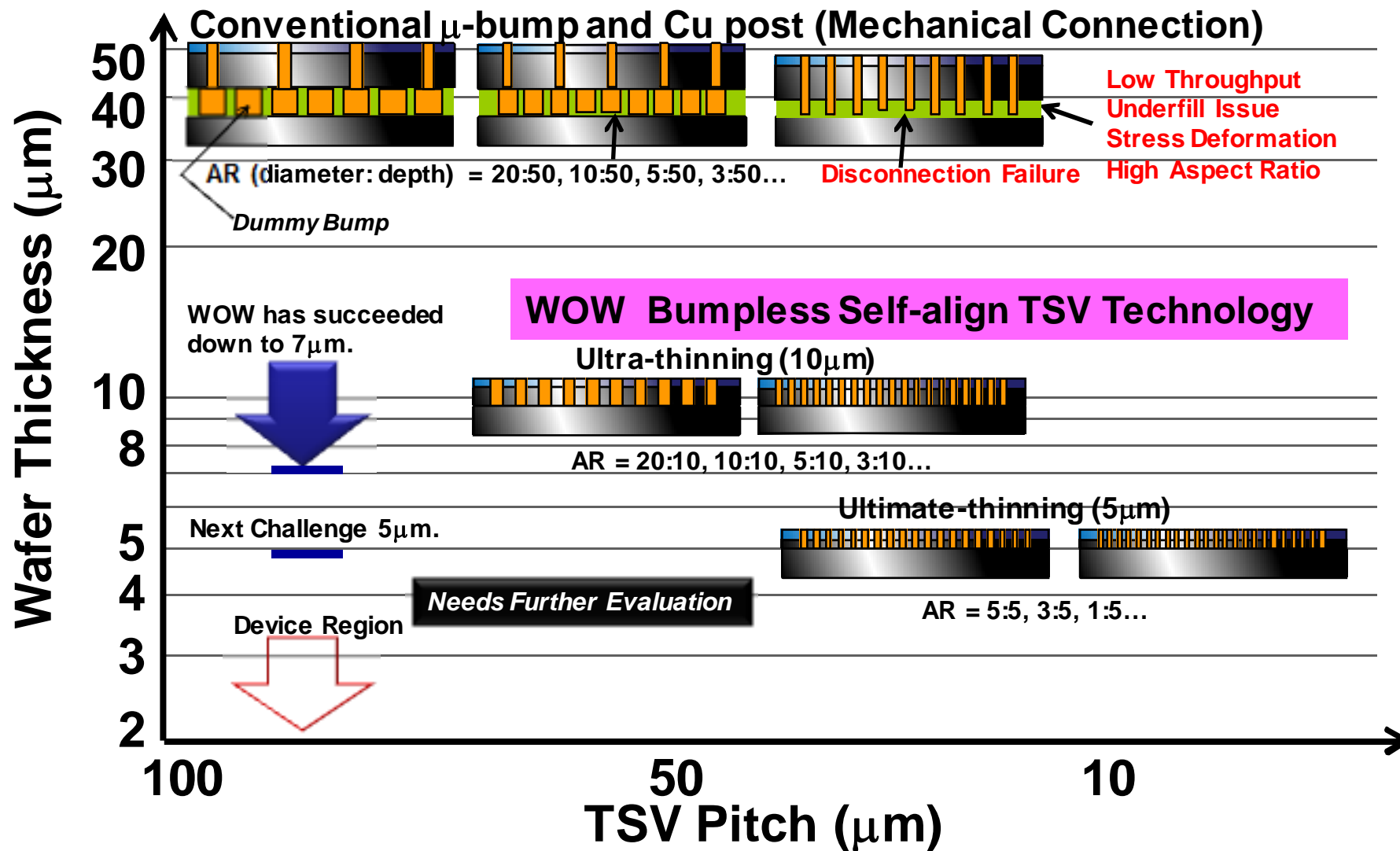


Cross-Sectional View of Si Substrate



Cross-sectional TEM image of Si substrate after thinning from the backside using Back Grind (Post BG), BG + Ultra-Poligrind (Post UPG), BG + Chemical Mechanical Polish (Post CMP), and BG + Dry Polish (Post DP), respectively.

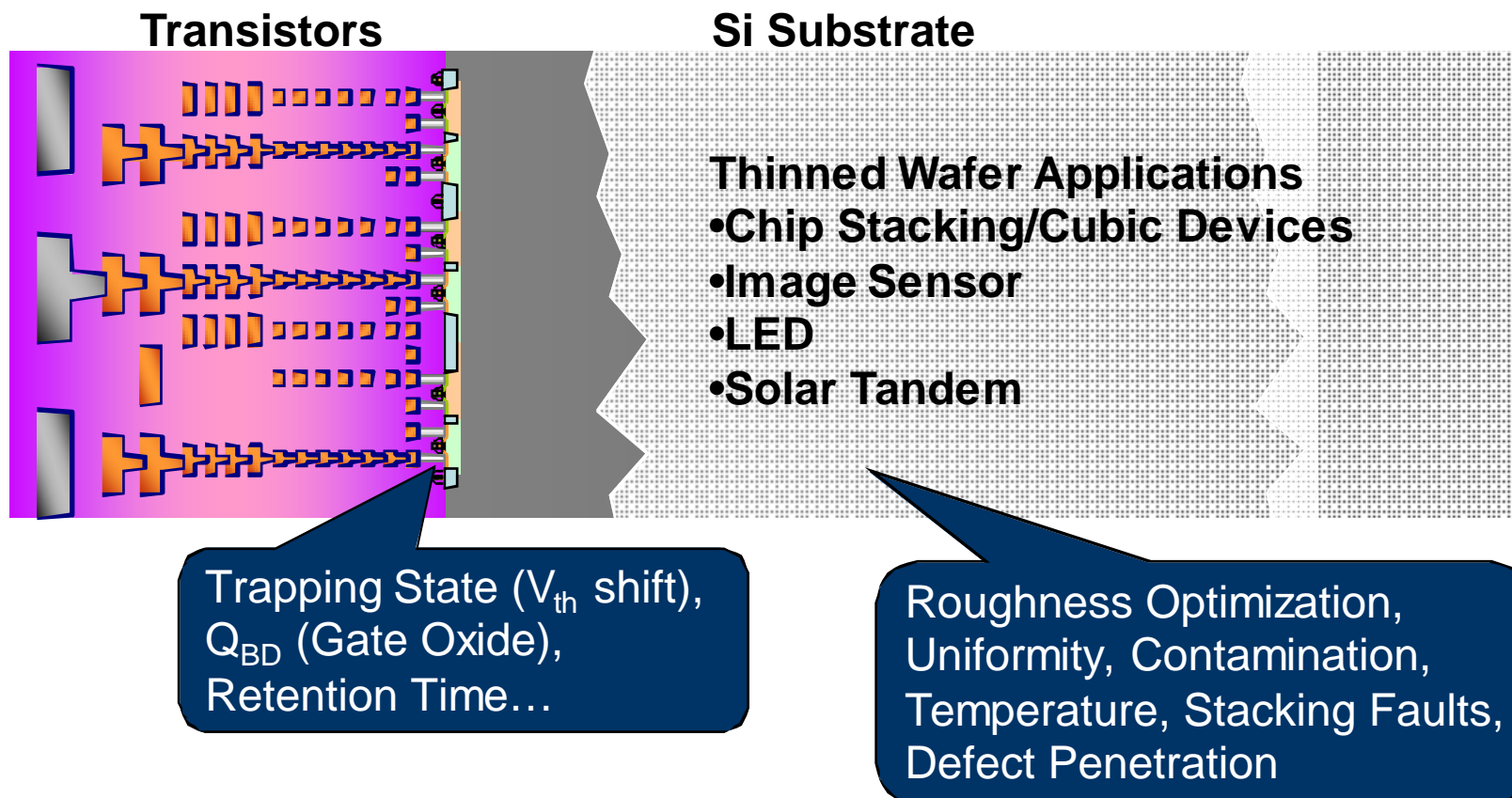
Roadmap of Wafer Thickness



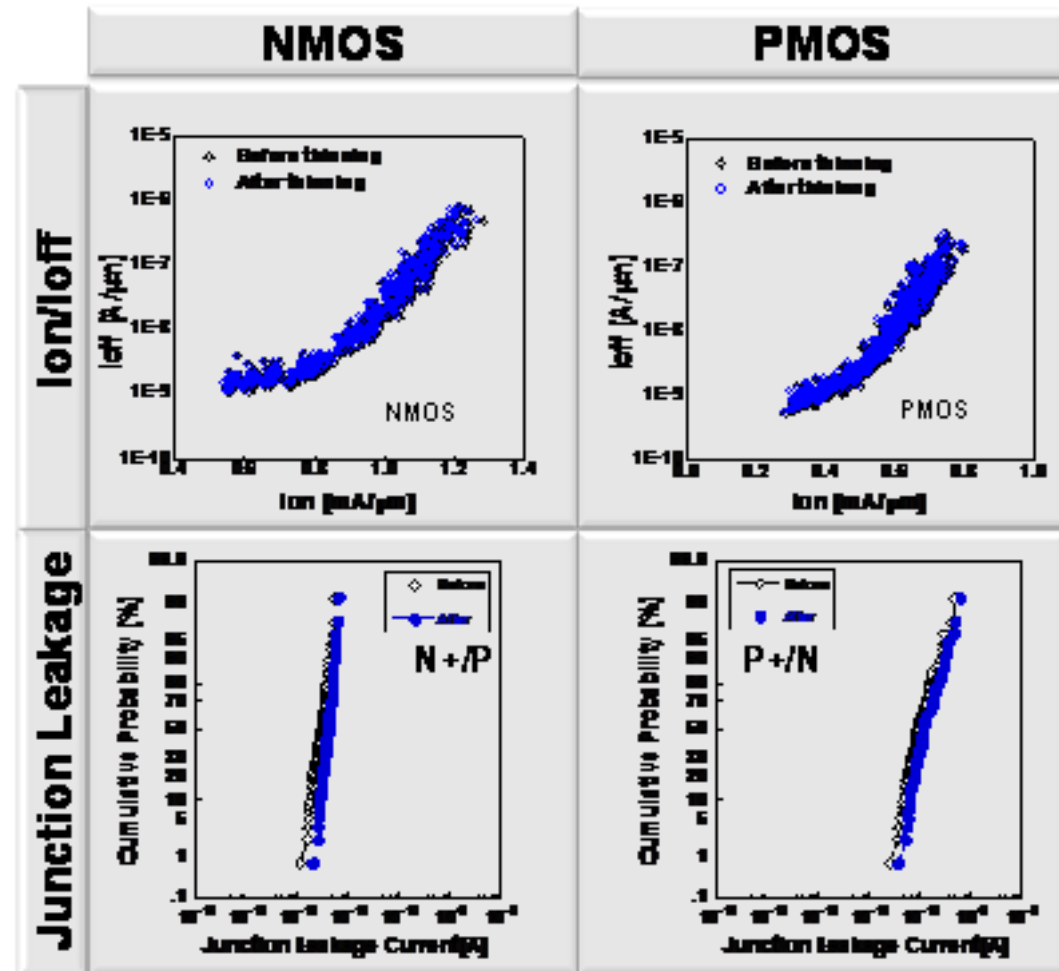
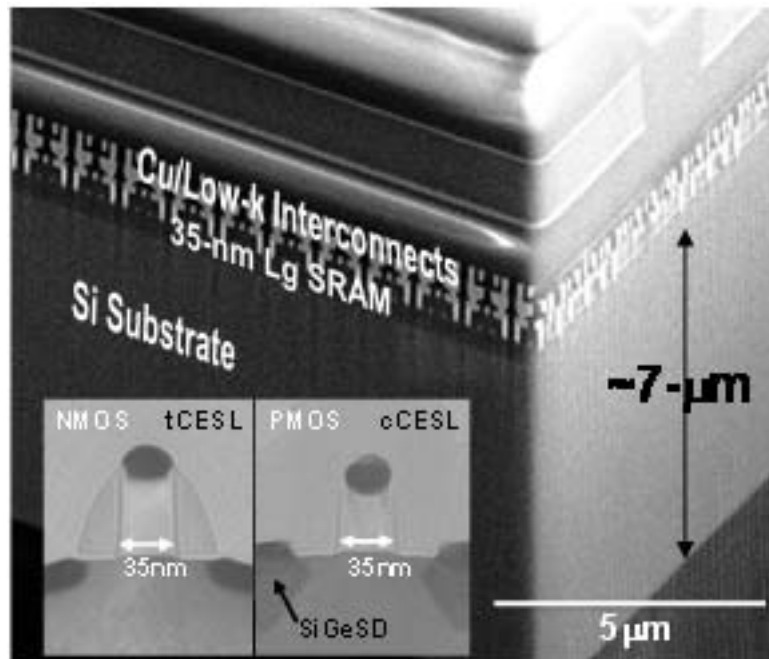
Further Evaluation for the Ultra-Thinning

Default = 10 μ m

Target ~ 5 μ m



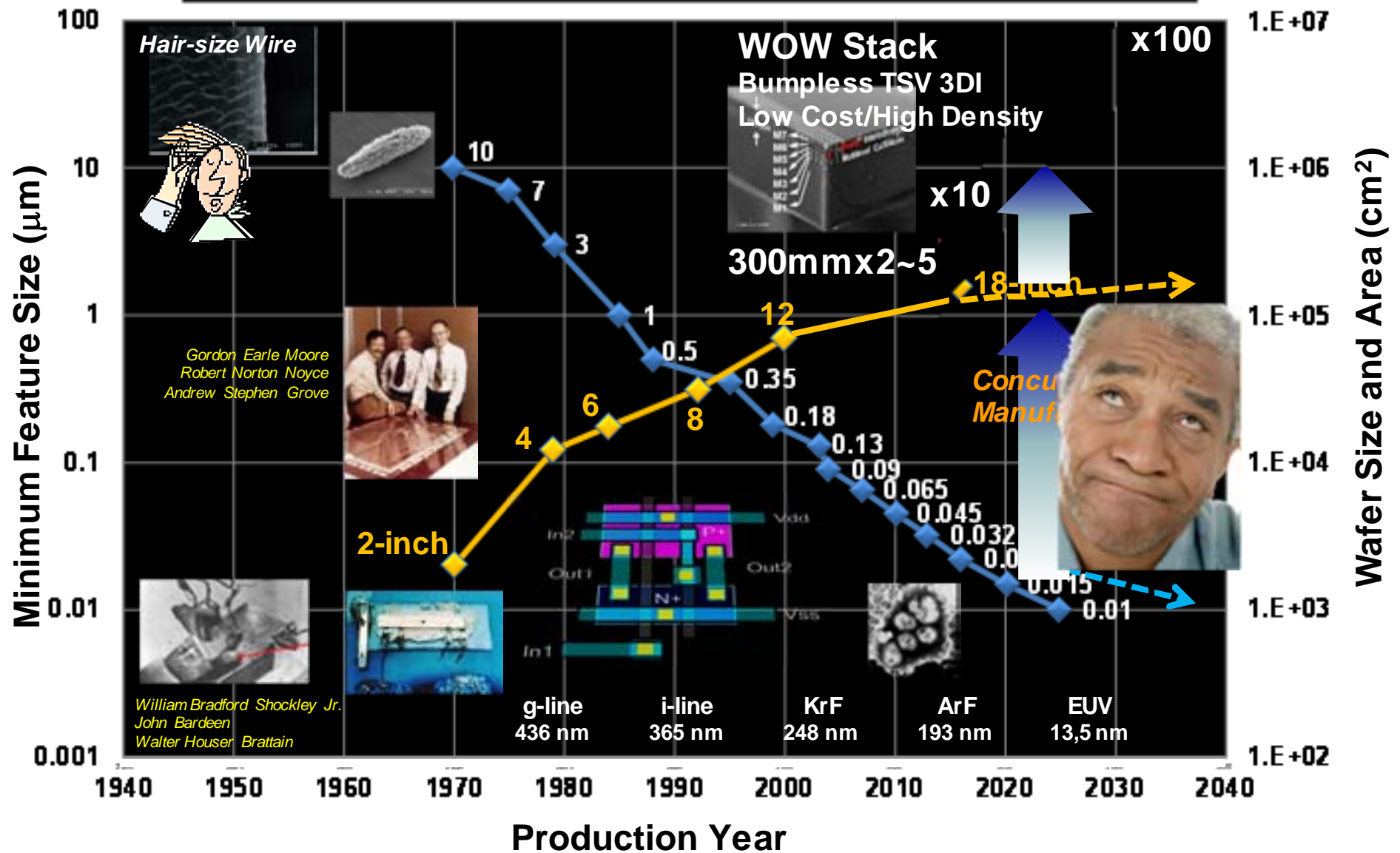
Thinned down to 7- μm using 45nm Node MPU



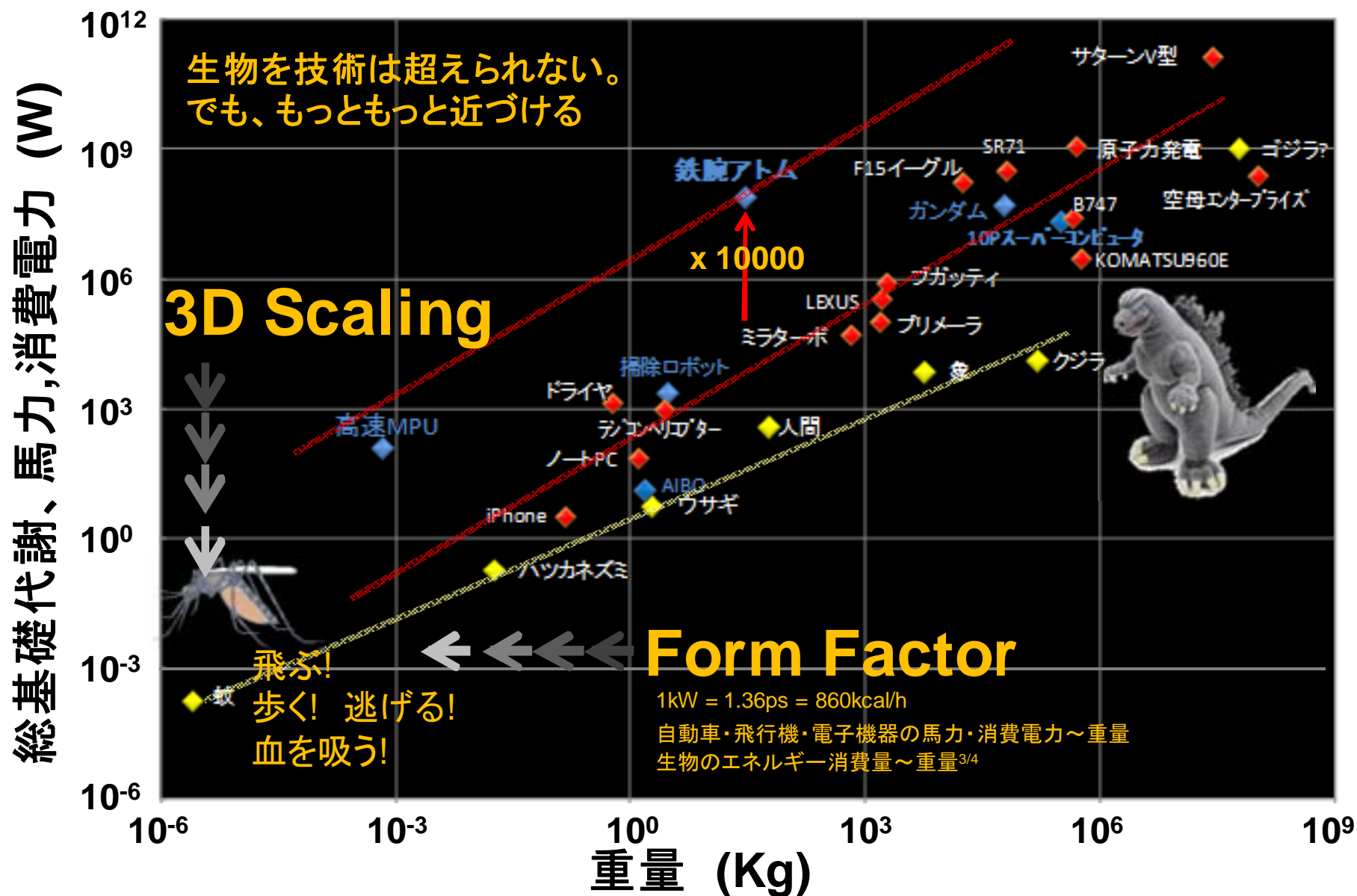
Cross-sectional SEM image of 300 mm wafer containing 35 nm-gate-length SRAM logic devices, thinned to 7 μm .

Kim et. al., IEDM 2009

History and Future in Semiconductor



やはり生物に学ぼう



Conclusions

- **Bridging tool and architectures**
 - **2D to 3D**
 - **Chip to Wafer**
 - **PKG to Front-end processing**
- **3D will become main stream later than 2015.**
- **Japan has opportunities if we could change.**

Acknowledgements

This study was carried out based on the three-dimensional integration development program of the WOW Alliance at the University of Tokyo, and the author thanks the more than 20 alliance members, including Nagoya University, ITRI Ad-STAC (Taiwan), and the WOW Research Center Ltd. for their cooperation.

安靜地聽謝謝

