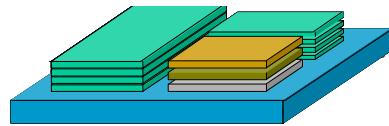


【主催】技術研究組合

超先端電子技術開発機構(ASET)

【共催】独立行政法人

新エネルギー・産業技術総合開発機構(NEDO)



ドリームチップ

平成23年度 研究成果報告会

パネルディスカッション

コーディネータ：傳田 精一 先生

パネリスト : 小柳 光正 先生

桜井 貴康 先生

池田 博明 ASET研究部長

Dream Chip Project Panel Discussion

Domestic OSAT
TSV main stream
TSV 3D Device

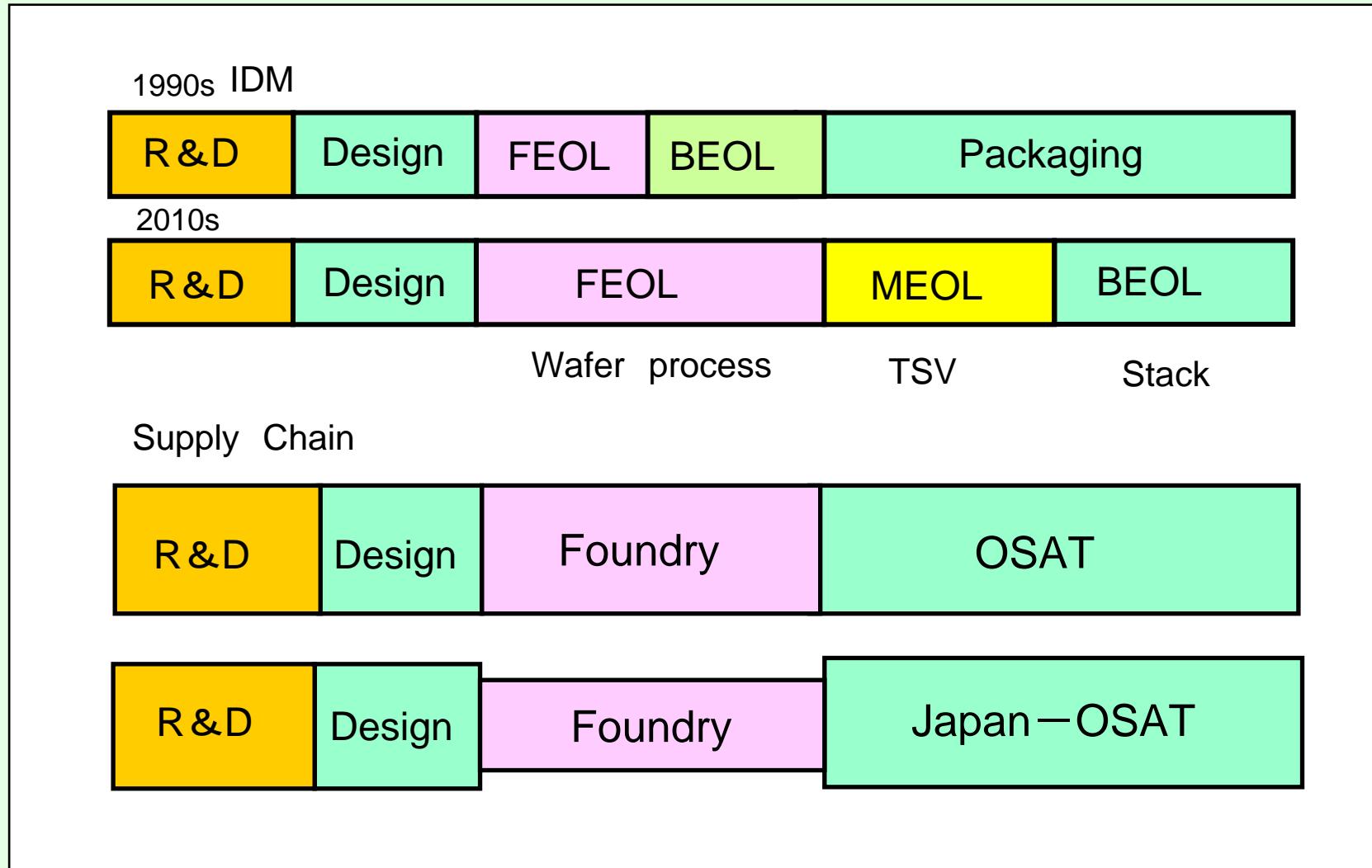
Dr. S. Denda

Nagano Prefectural Institute of Technology
Nagano Jisso Forum

June 6.26, 2012



3D Semiconductor Supply Chain



Can Domestic OSAT Grow up?

Powerful supports for 3D

- Vacuum Equipment
- Cu via Plating
- Wafer Dicing
- Wafer Thining
- CMP
- Wafer Handling
- Polymer Materials
- Die Bonding
- Organic Substrate

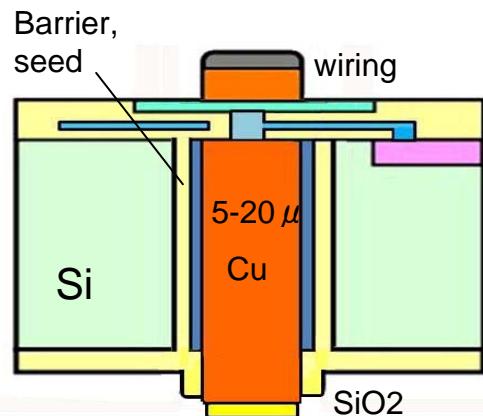


Ion etcher



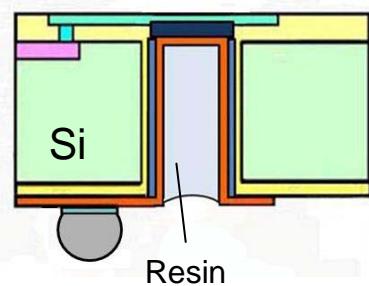
Via filling

Typical via structure

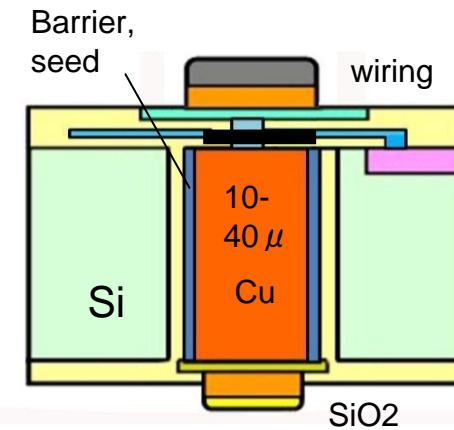


Via Middle
(Cu filling via)
Suitable for foundry

Temperature:400°C



Via last-back
(Cu conformal)
Sensor,
MEMS

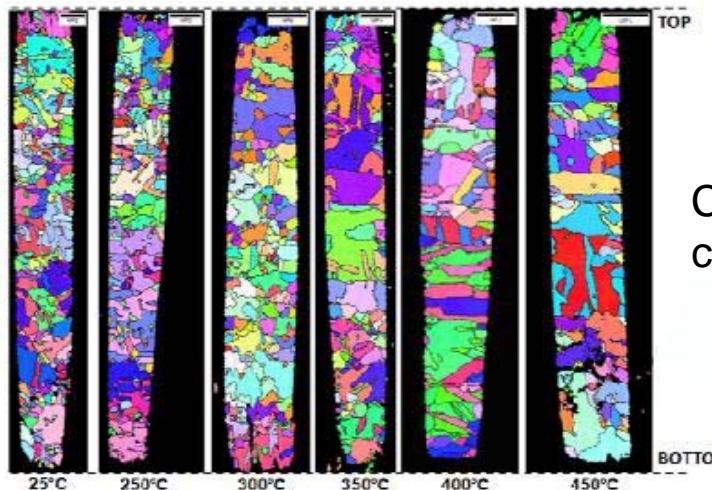


Via last-back
(Cu filling via)
Suitable for packaging
firm (OSAT)

Temperature:200°C

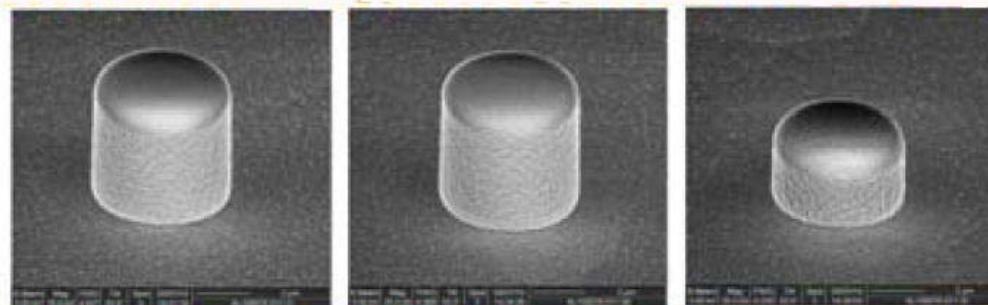
Problems in via middle process

Via protrusion



Crystal size
change

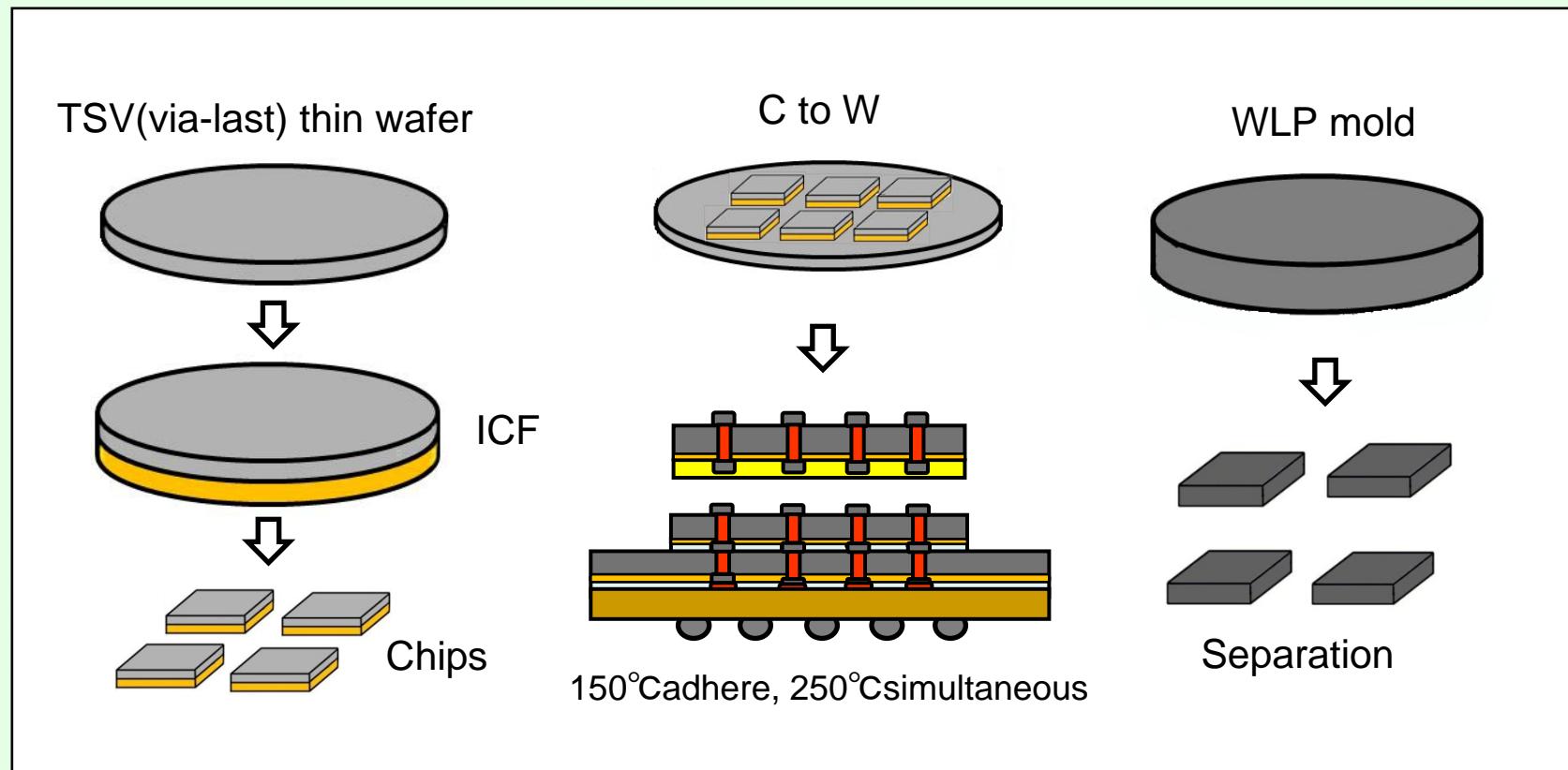
Backside reveal



300mm
Wafer ,
TSV dia
5 μ m

C to W hybrid bonding, with ICF and WLP

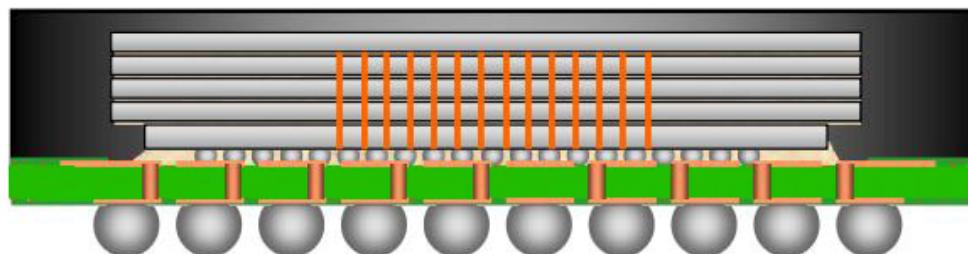
Mainstream for TSV-3D devices
Thin wafer, fine pitch, multi bump, low cost



Requirement: new materials, support system, handling, dicer, bonder

Comment on TSV Products—Wide I/O DRAM

Big demand for smartphone DRAM
512 bus width (1,200bumps)^① in 2013
4K bus width (~8,500bumps)^②
For more than 4K, larger chip size and
excessive connections

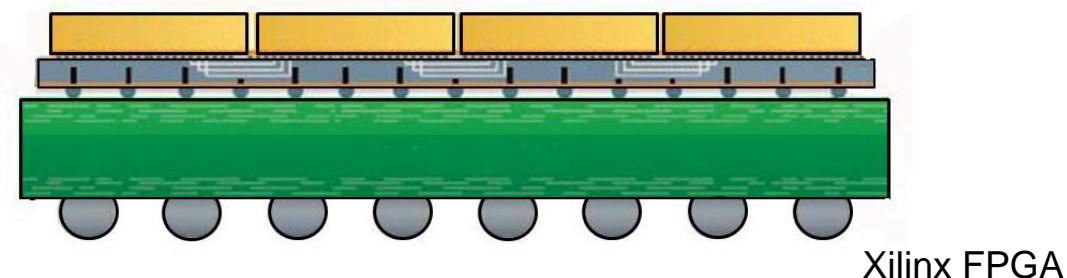


JEDEC JESD229

①JEDEC ②ASET

Comment on TSV products – 2.5D device

Homogeneous and heterogeneous
Thin Si interposer
Warpage takes place
Thick interposer
Higher performance, higher cost



END

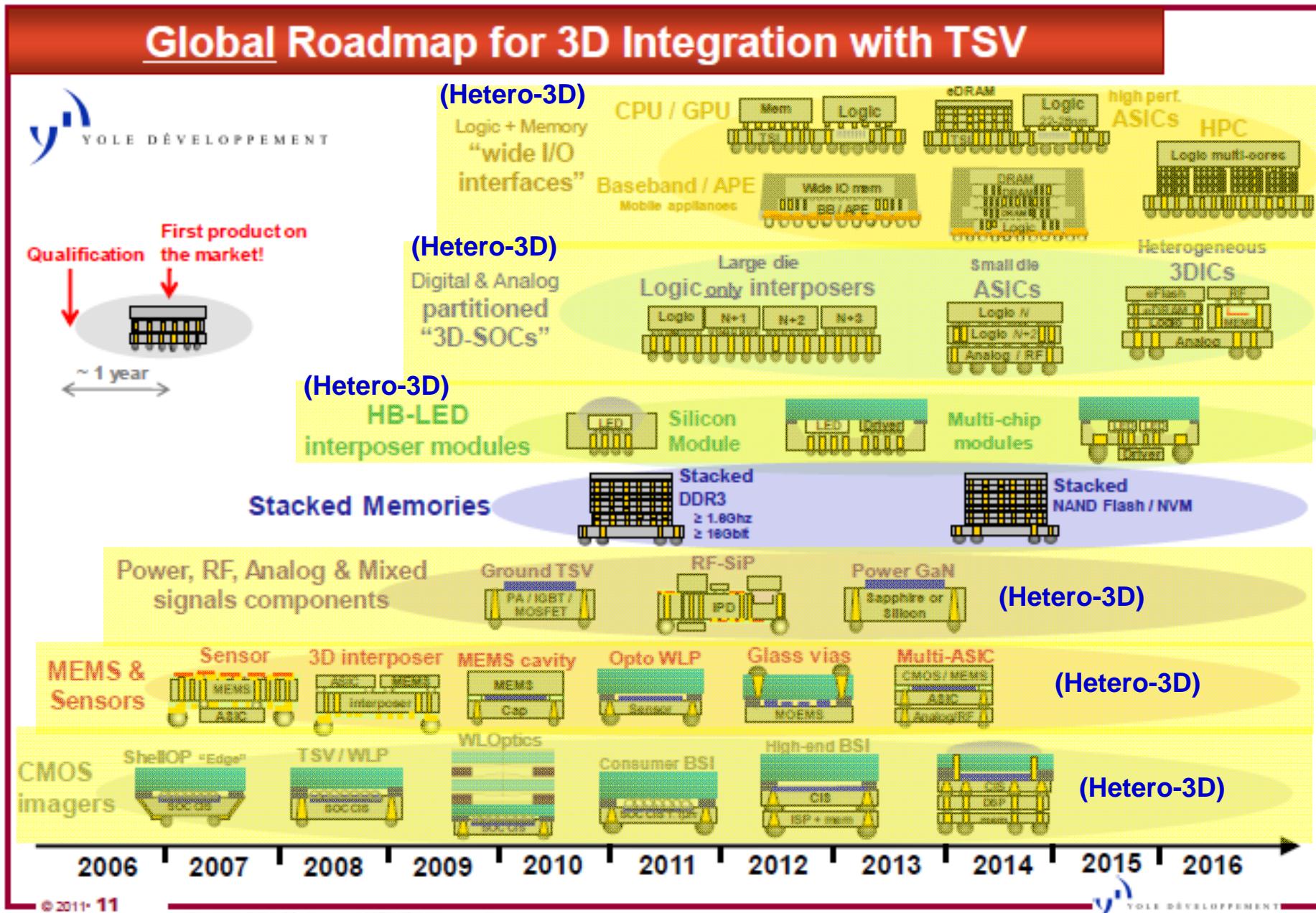
Dream Chip Project Panel Discussion



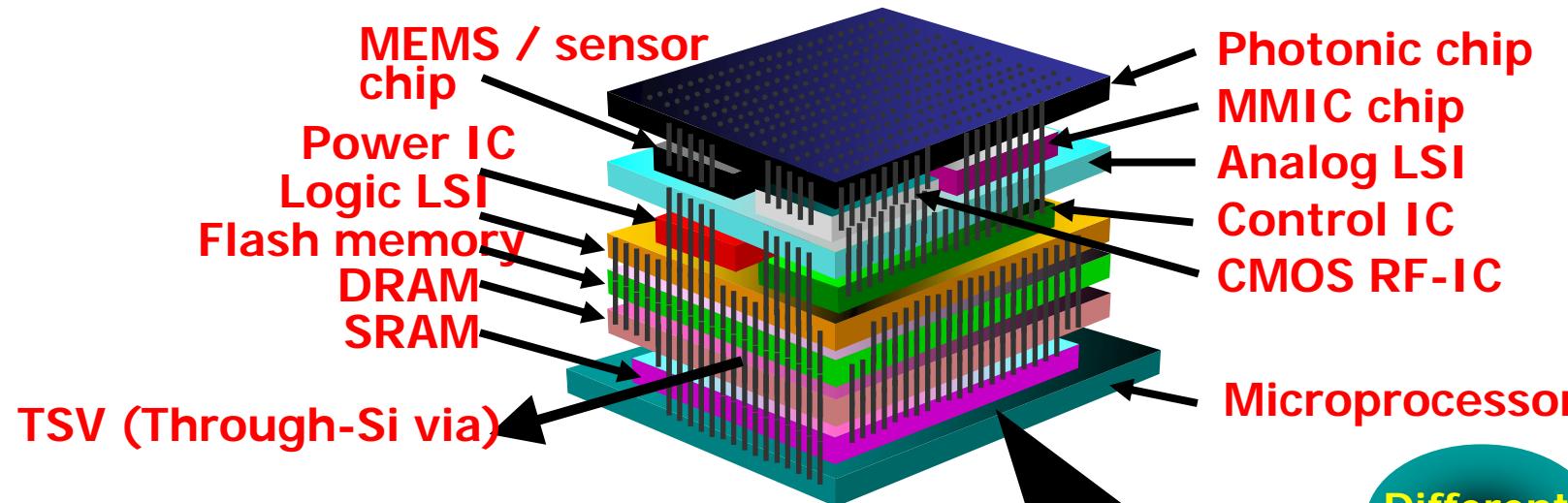
Design and Test Issues In Heterogeneous 3D-LSI

Mitsu Koyanagi

New Industry Creation Hatchery Center
Tohoku University
Sendai, Japan

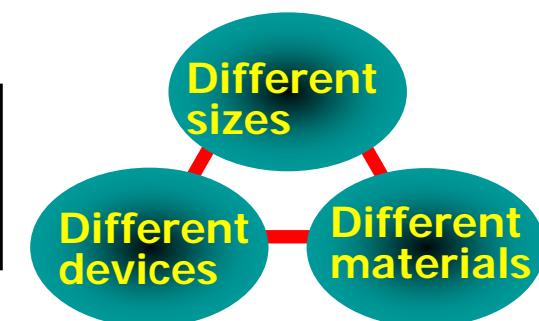


Heterogeneous 3D System Integration Projects in Tohoku University

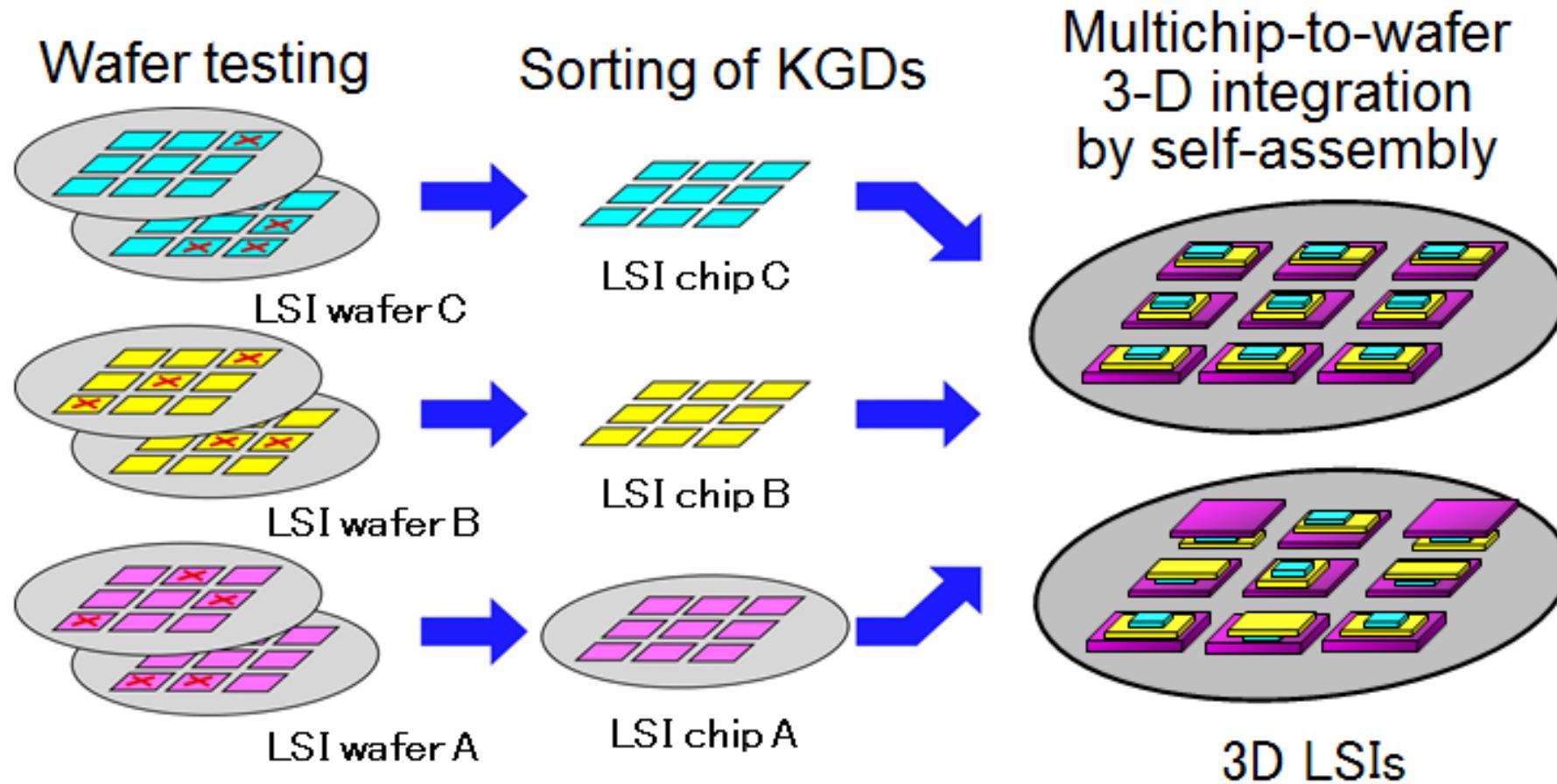


**3D Super
Chip**

- 1999(IEDM): 3D Image Sensor
- 2000(IEDM): 3D Shared Memory
- 2001(ISSCC): 3D Artificial Retina
- 2002(Cool chips): 3D Microprocessor
- 2005(IEDM): Super Chip Integration, Self-Assembly, 10-Layers Memory
- 2007(IEDM): Reconfigured Wafer-on-Wafer 3D Integration, Self-Assembly
- 2008(IEDM): Heterogeneous Multi-Chip Module (LSI-MEMS)
- 2009(IEDM): Wafer-thinning and back-metal contamination in 3D-LSI
- 2010(IEDM): Interconnects induced thermo-mechanical stress
- 2011(IEDM): W/Cu hybrid TSVs and 3D-LSI



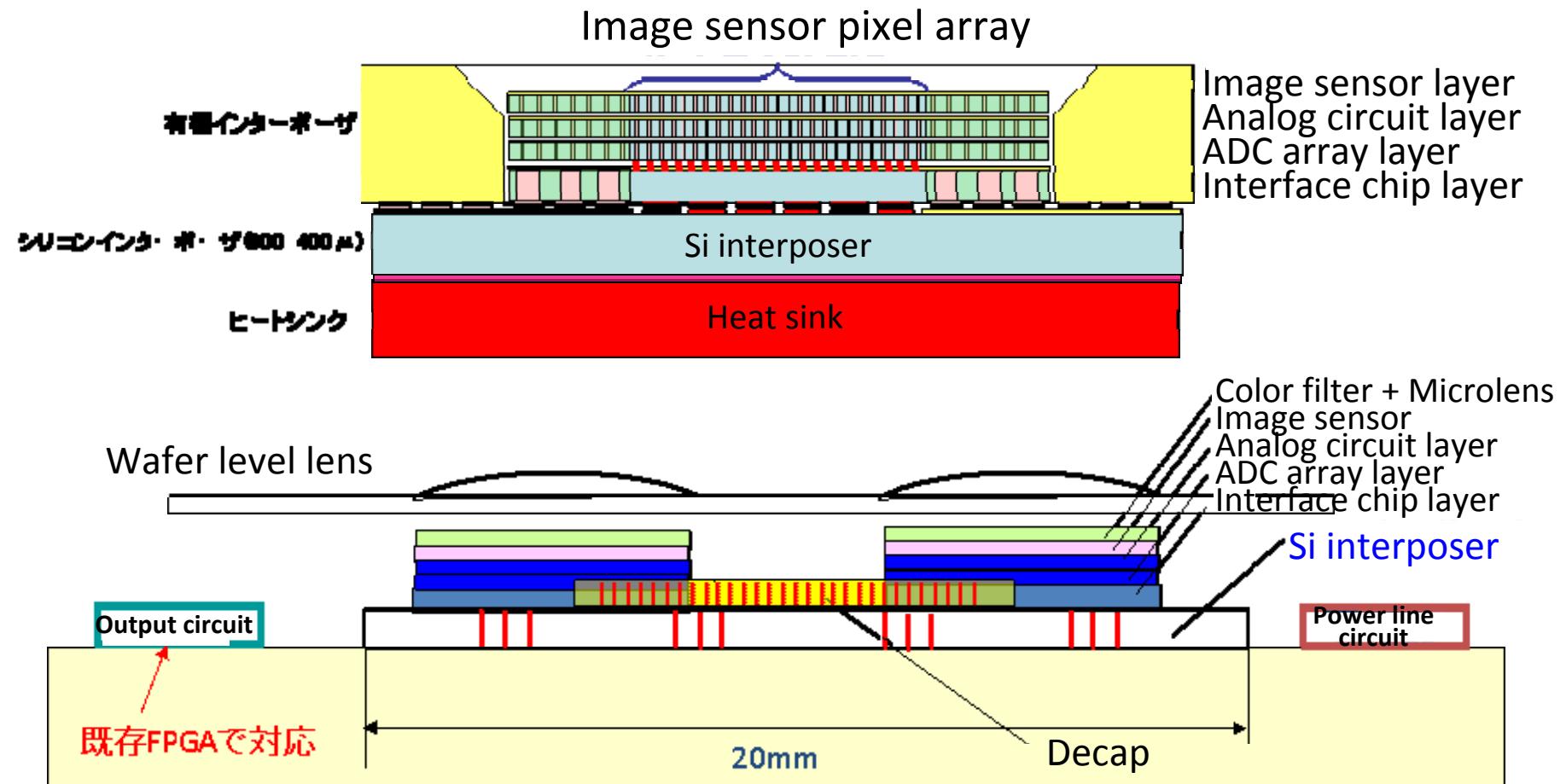
Super-Chip Fabrication by Multichip-to-Wafer Bonding



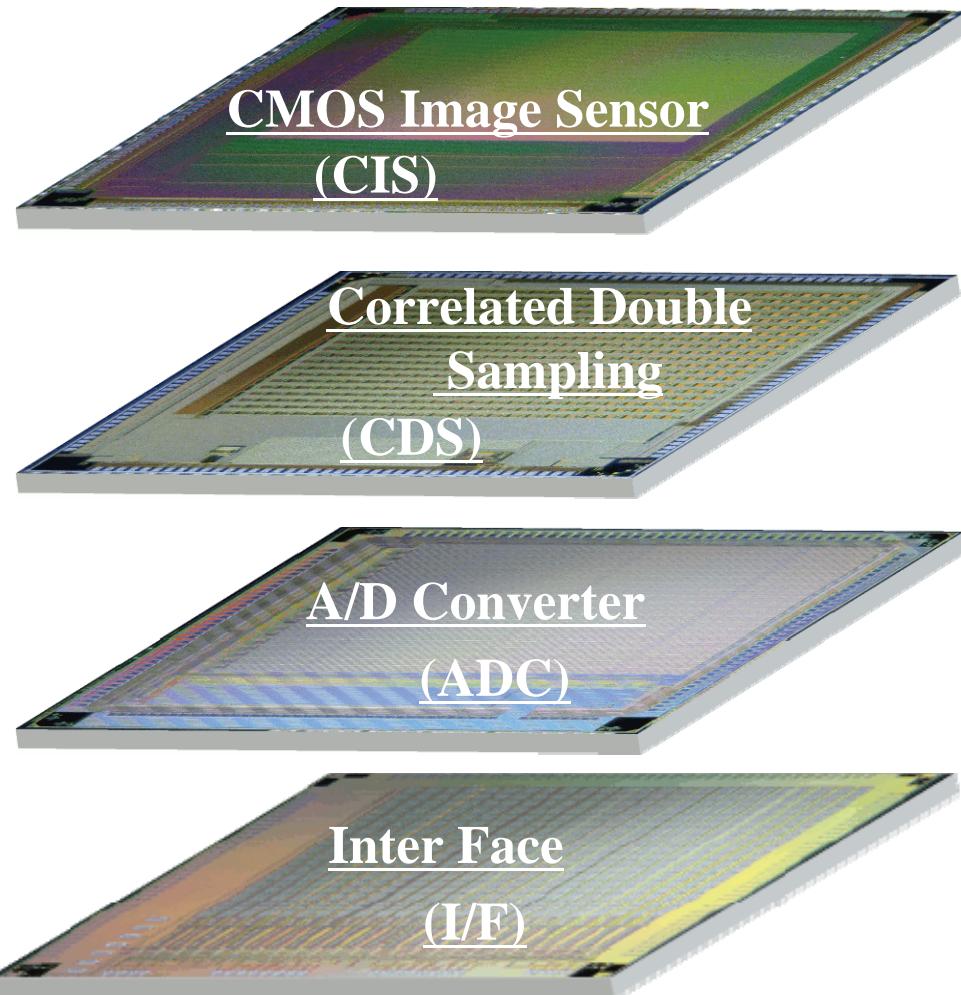
Example of Heterogeneous 3D-LSI

Digital-Analog Mixed Signal 3D-LSI

3D-Stacked Image Sensor Chip (NEDO/ASET Dream Chip Project)



Configuration of 3D stacked LSI



1st layer : CIS chip

180nm 1-Poly 6-Metal CMOS
Image sensor technology

2nd layer : CDS chip

180nm 1-Poly 6-Metal CMOS
Mixed signal technology

3rd layer : ADC chip

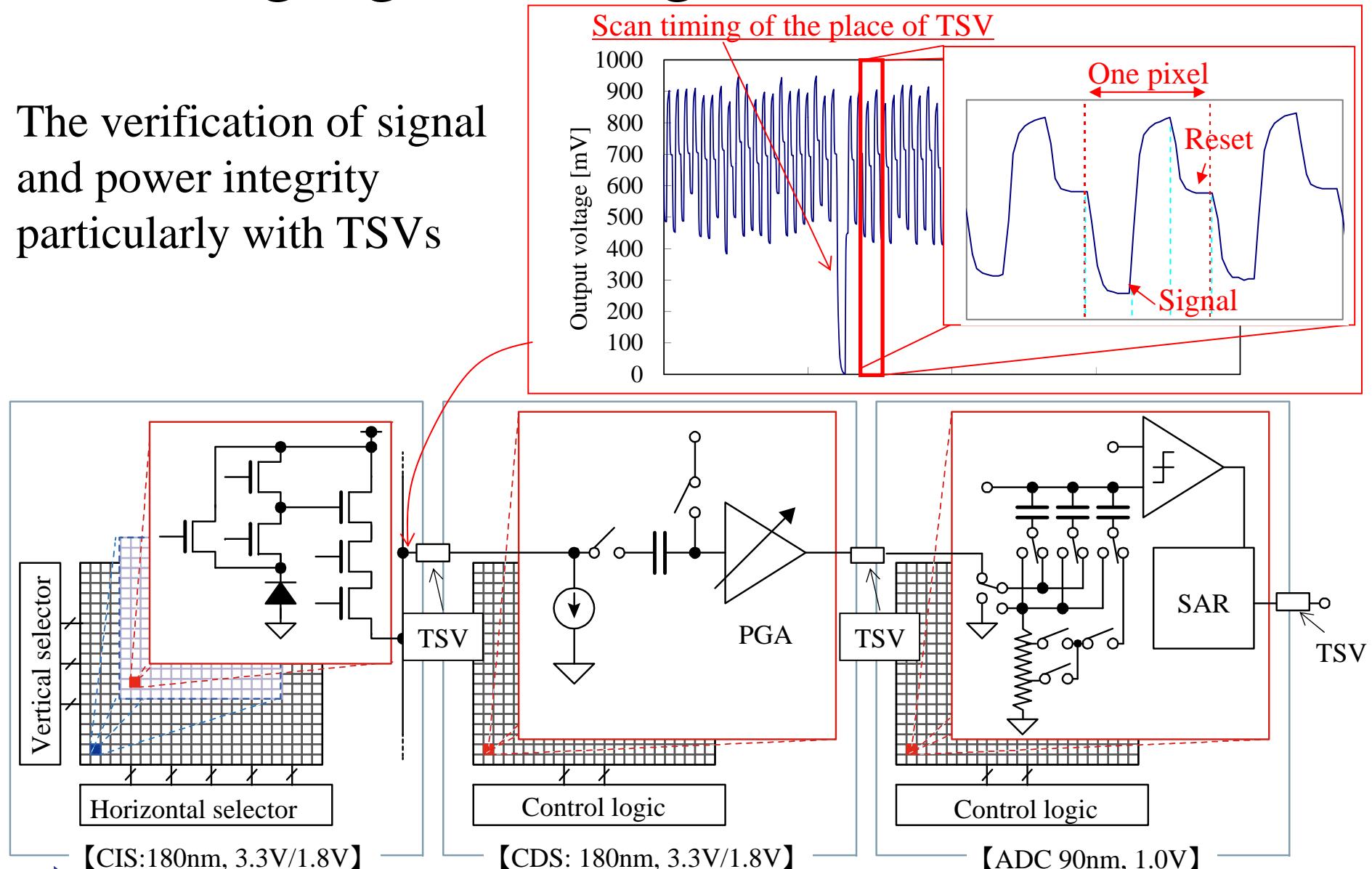
90nm 1-Poly 9-Metal CMOS
Mixed signal technology

4th layer : I/F chip

130nm 1-Poly 8-Metal CMOS
Logic technology

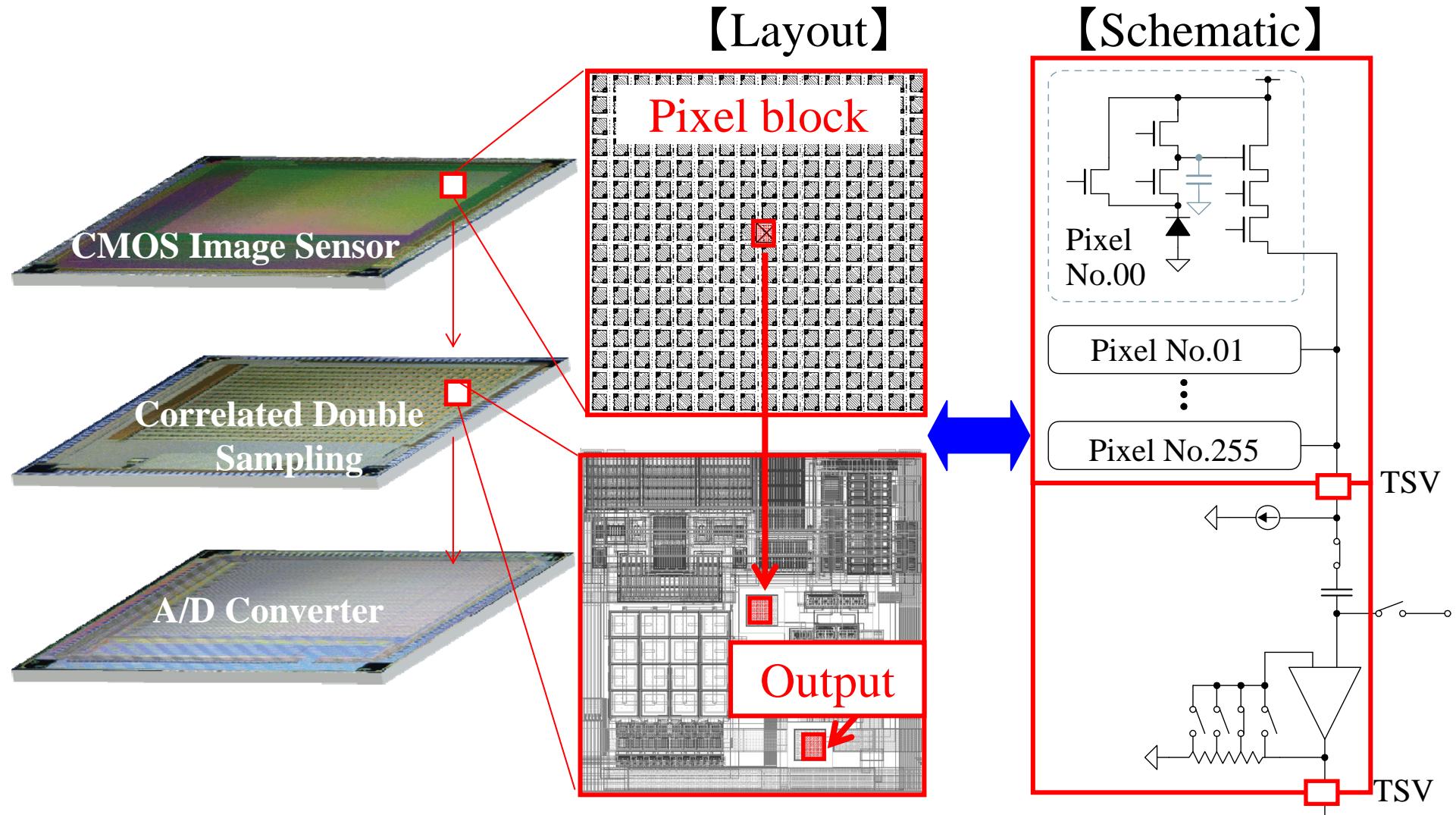
Emerging challenges for simulations

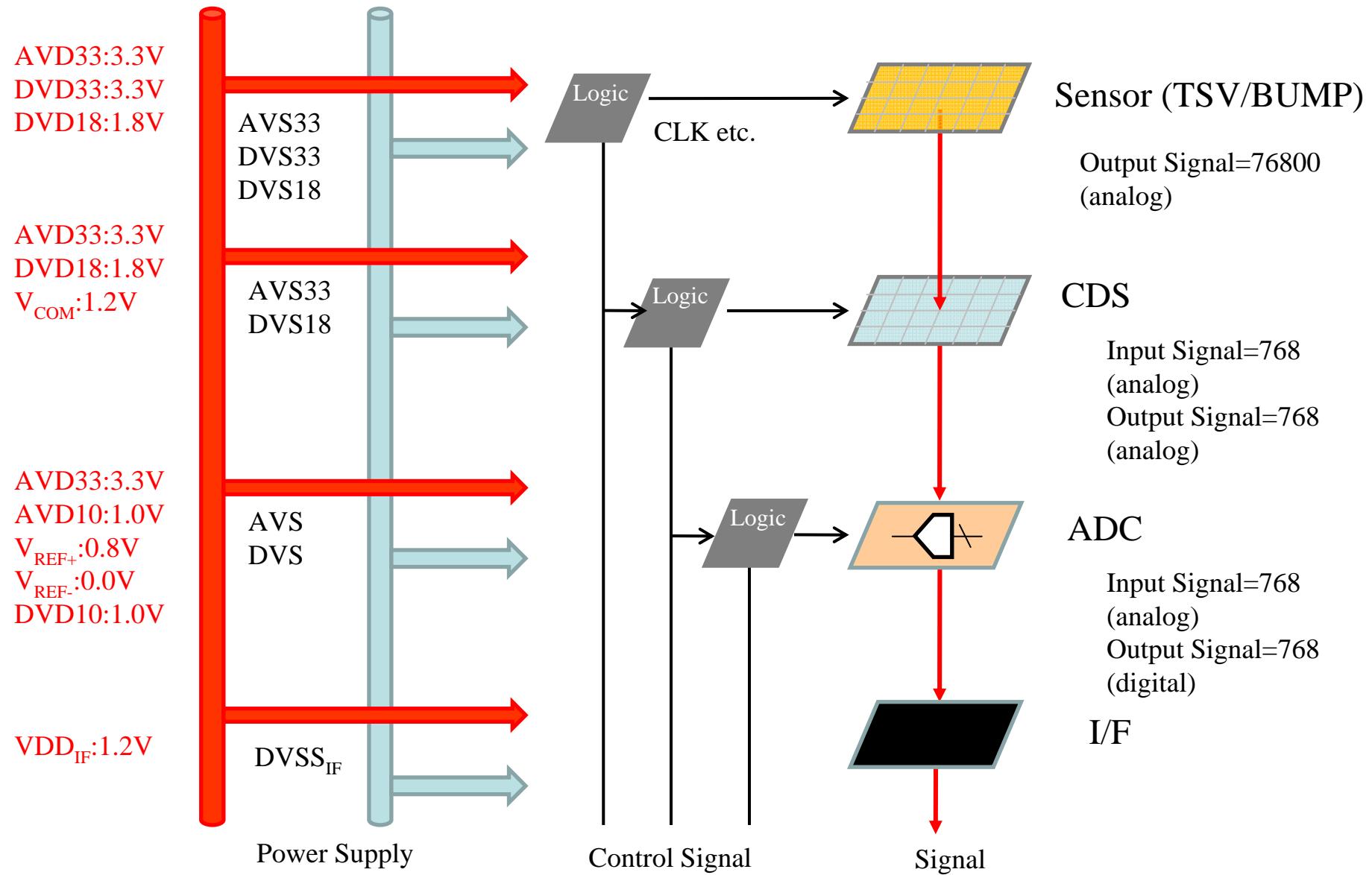
The verification of signal and power integrity particularly with TSVs

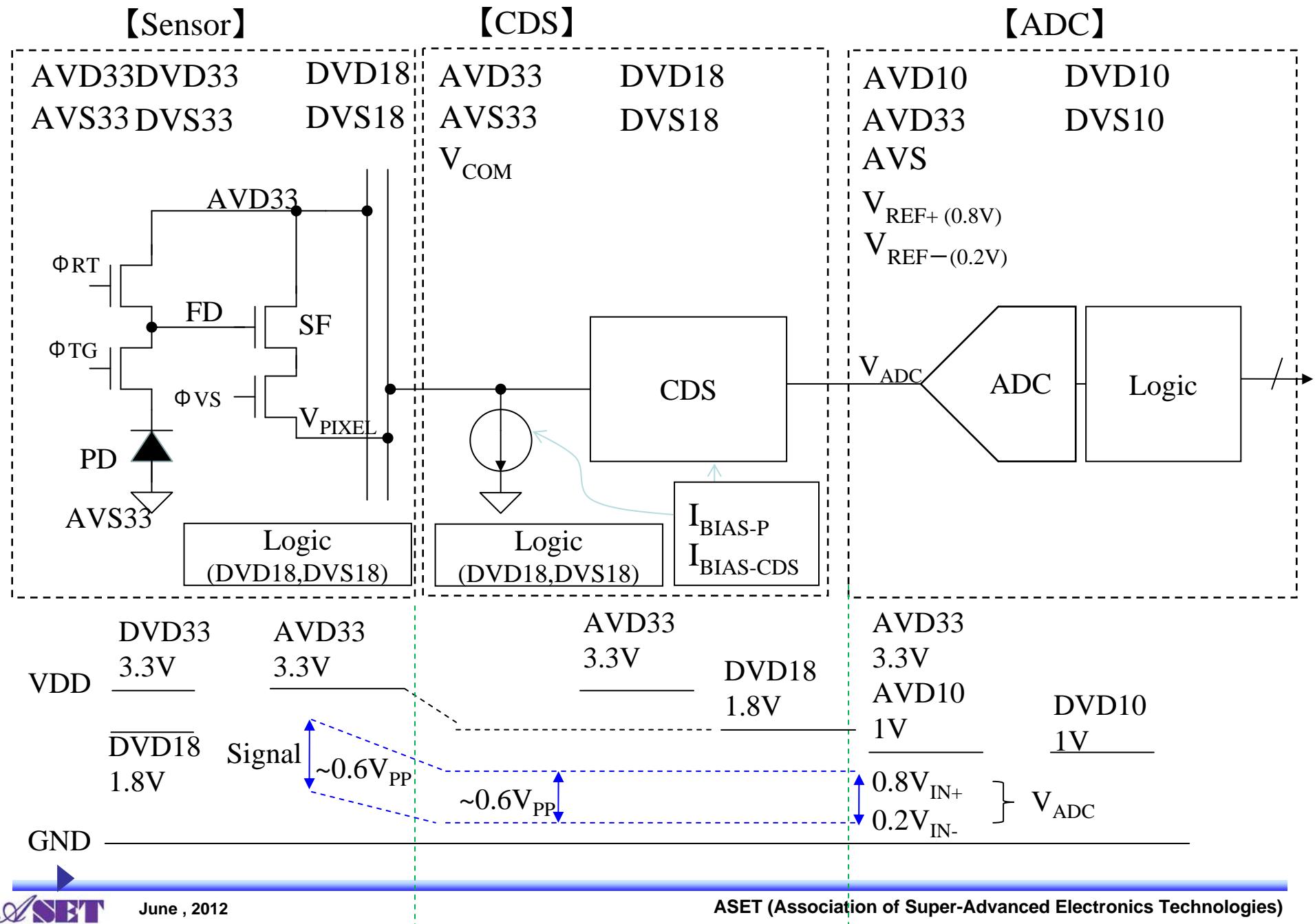


Verification techniques are needed

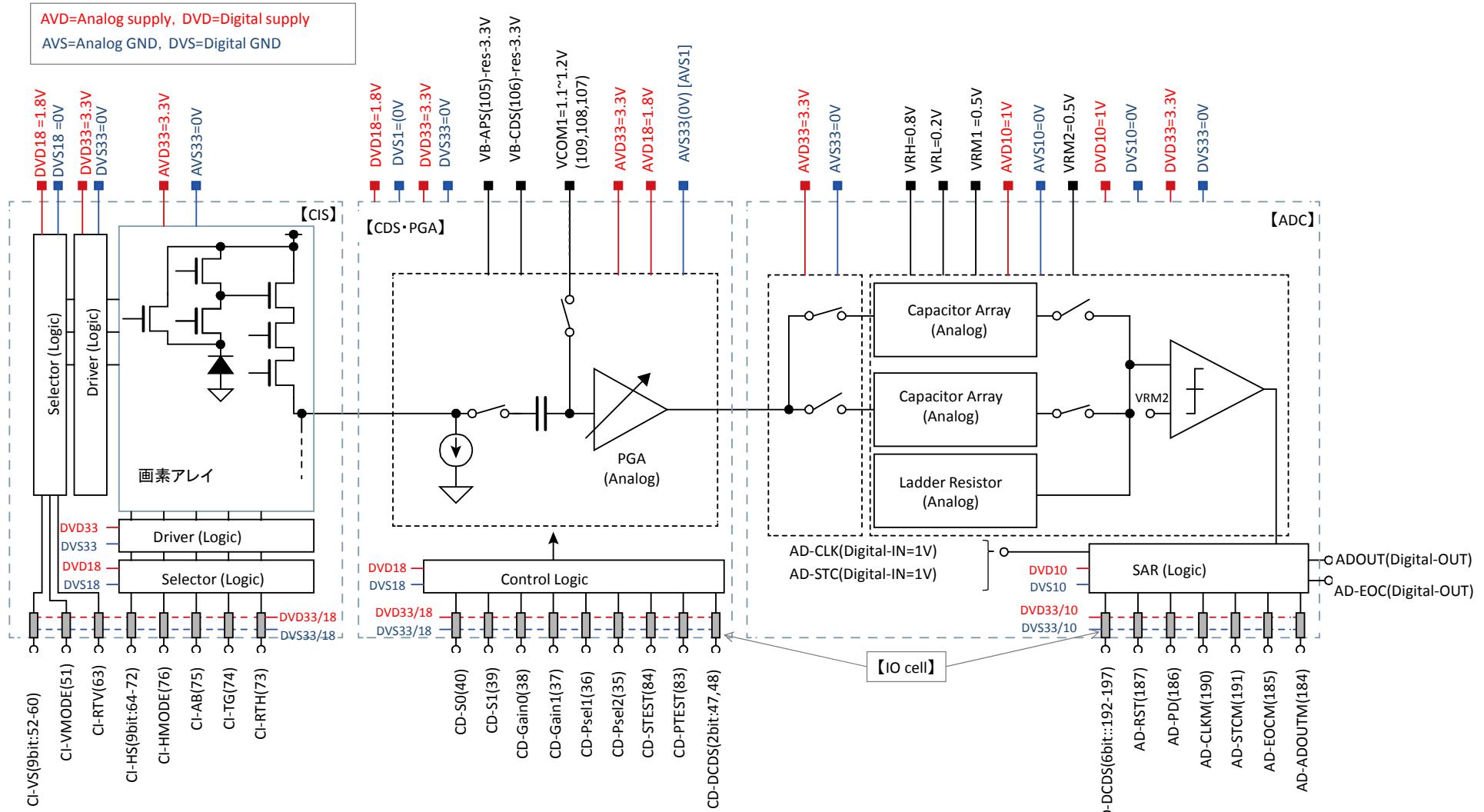
3D stacked verification includes DRC, ERC and LVS





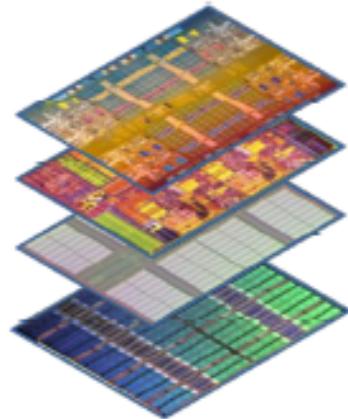


Block diagram and terminals



Compute / Network / Graphics

Heterogeneous Digital



High Performance
Low Power/Accelerator
Specialized RAM
General RAM

Codesign

- Different companies
- Different fabs
- Sequential design
- Plug and Play

Power Delivery

- Future proofing

Signaling

- Future proofing

Thermal Control

- Without parallel codesign

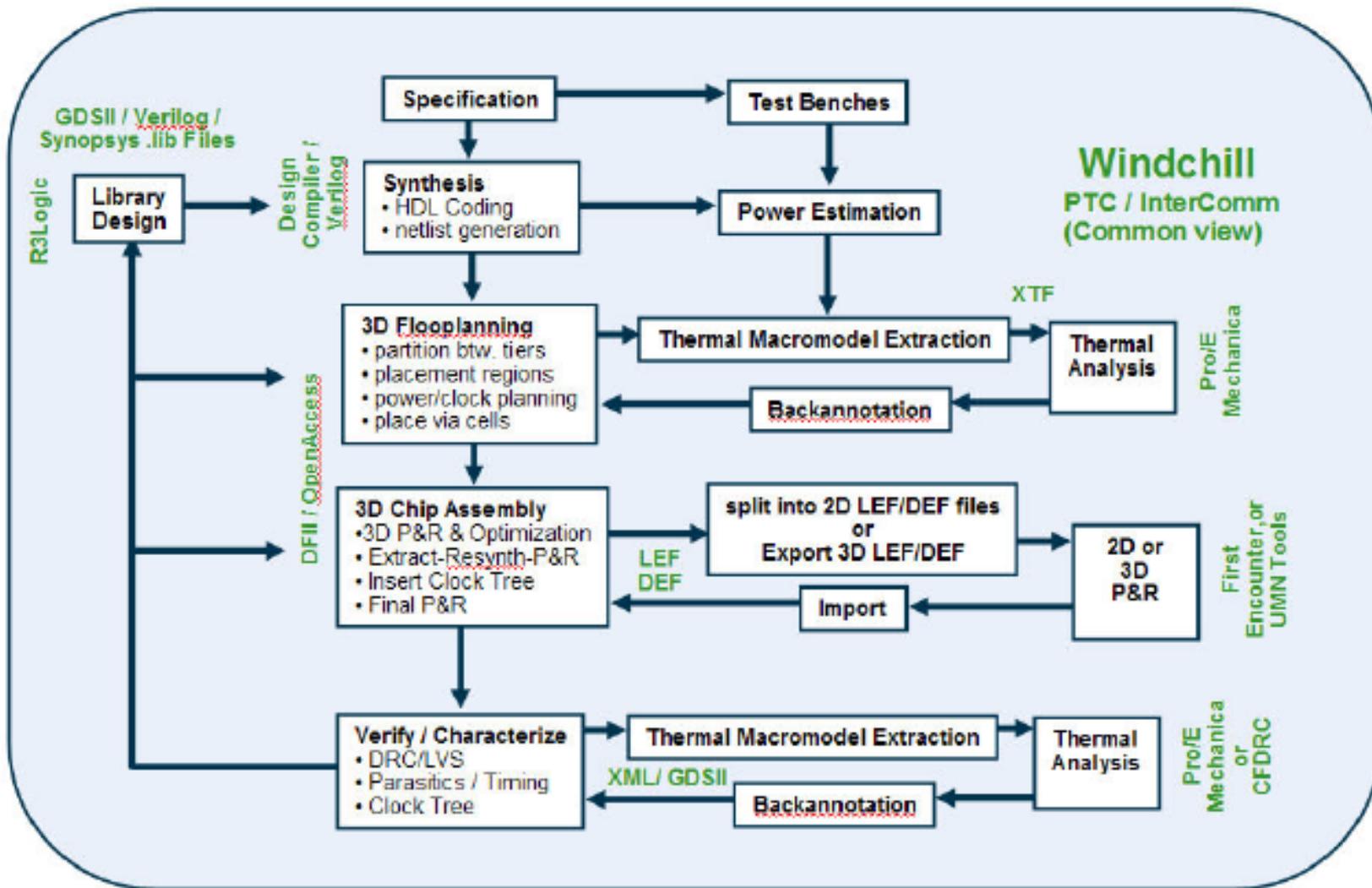
After P. Franzon (NCSU) 3DIC 2011, Osaka

The “issues” to be resolved

- Signaling
- Timing
- Power Delivery – DC
- Power Delivery – AC (i.e. Noise)
- Thermal control
- Physical integration technology
- Redundancy management
- Test and Validation support
- Integration with CAD
- CAD interchange

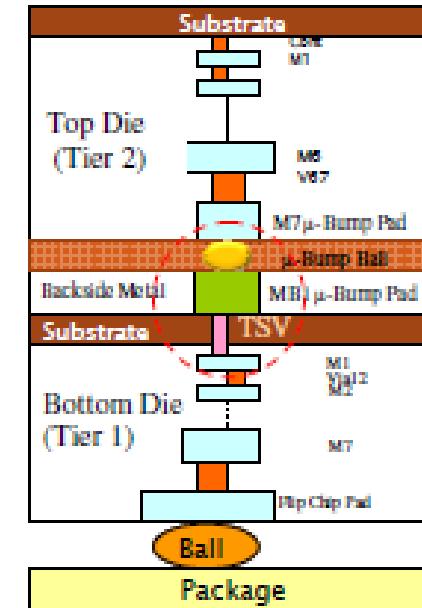
After P. Franzon (NCSU) 3DIC 2011, Osaka

3D Design Flow in NC State University (True 3D Flow)



3D Technology & Design Kit

- Target technology
 - Uses ST-Microelectronics high-speed CMOS library
 - Uses TSV middle ($\varnothing 10\mu\text{m}$) + Copper Pillar ($\varnothing 10\mu\text{m}$)
 - Is a Flip-Chip packaging assembly
 - Is a Face2Back, Die to Wafer 3D stacking assembly
- Back End kit
 - Virtuoso tech file addon kit for 3D layers
 - EDI Techno file & capturable
 - DRC & LVS « 3D » addon kit



RTI Conference - 18th Dec 2011
A Three-Layers 3D-IC Stack including WidelIO and 3D NoC

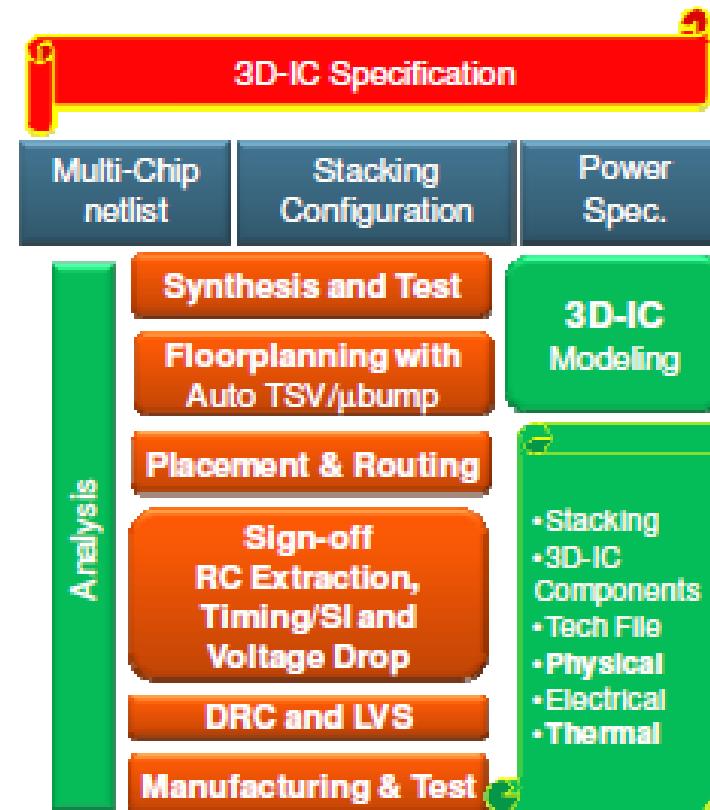
25

cadence  

After P. Vevet , 3D-Architecture 2011, San Francisco

EDI 3D-IC Stack Design Implementation & Analysis

- Cadence **Encounter 3D-IC** design implementation is developed in collaboration with major foundries and advanced system designers.
- Supports a comprehensive 3D-IC modeling for both implementation and analysis.
 - Different types of 3D Interconnect: TSV, micro-bump, copper pillar or direct bonding and backside metal layers.
 - Multiple set of manufacturing rules
- Supports multiple types of 3D-IC stacking in design implementation and analysis
 - Silicon interposer
 - Vertical stack.
 - Mixed stack.
- EDI Design methodology and design flow are proven with several 3D-IC tape-out.



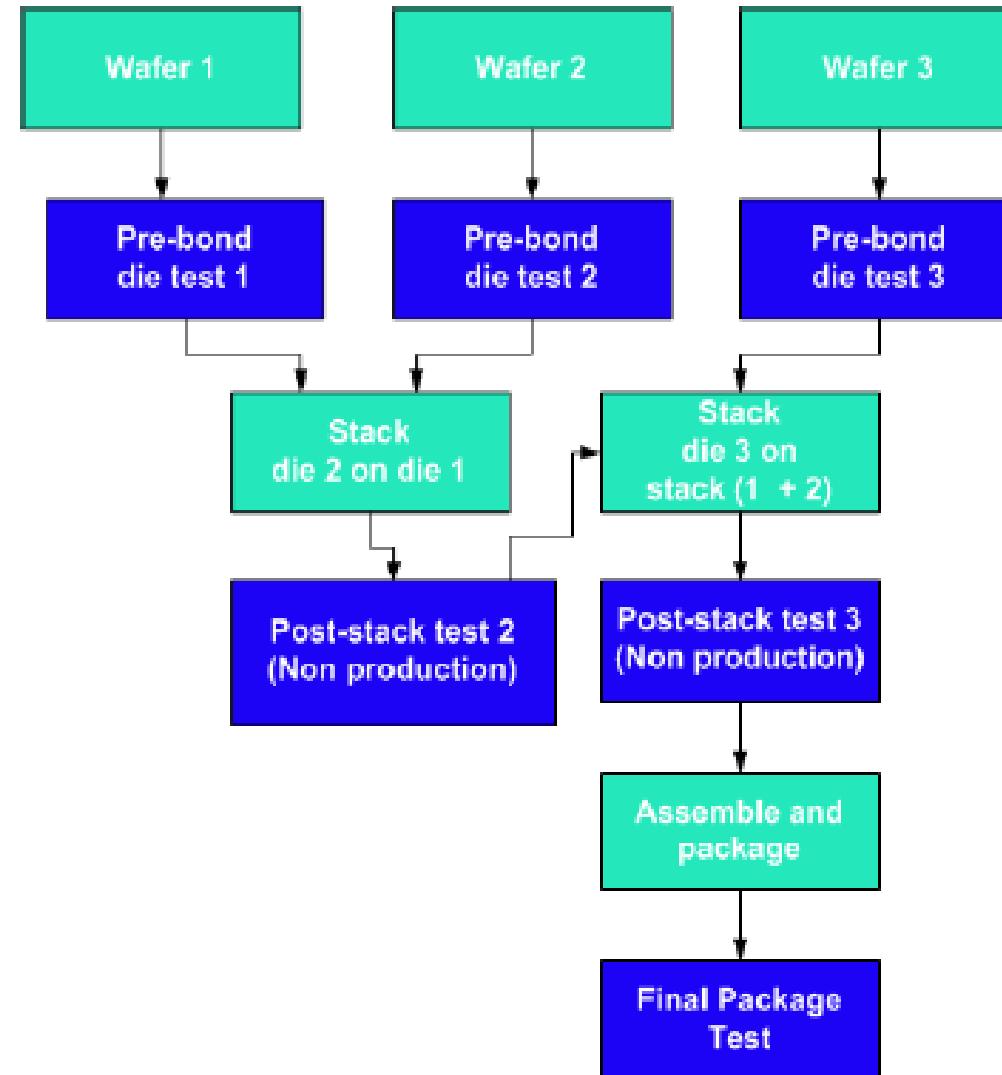
RTI Conference - 13th Dec 2011
A Three-Layers 3D-IC Stack including WidelO and 3D NoC

26

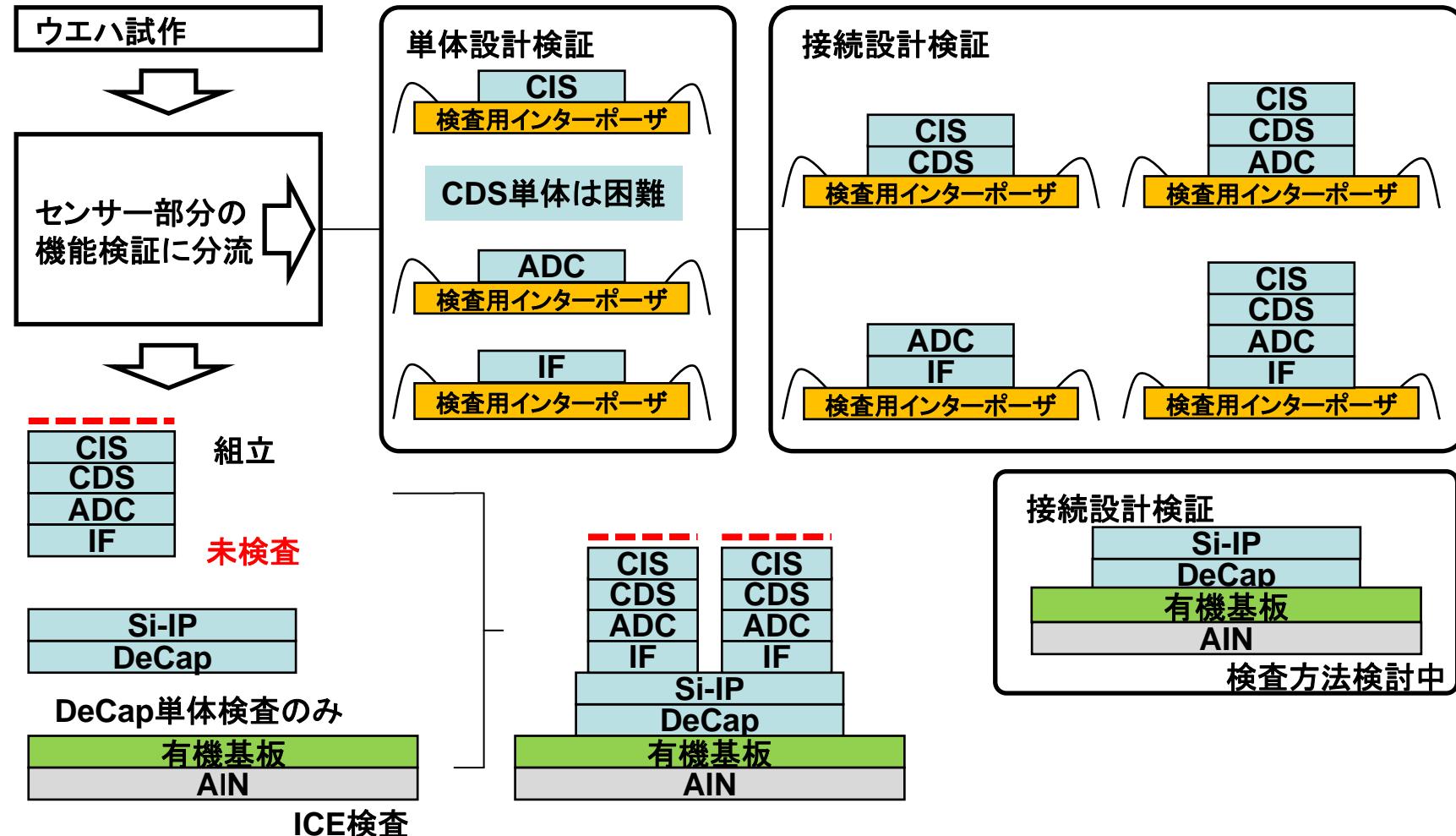


After P. Vevet , 3D-Architecture 2011, San Francisco

3D Test



3D Testing and DfT



鎌田資料 (ASET デジアナ混載WG)

3D DfT Architecture

Example Functional Design

- **≥2 stacked dies, possibly core-based**
- **Inter-connect: TSVs**
- **Extra-connect: pins**

Example Existing Design-for-Test

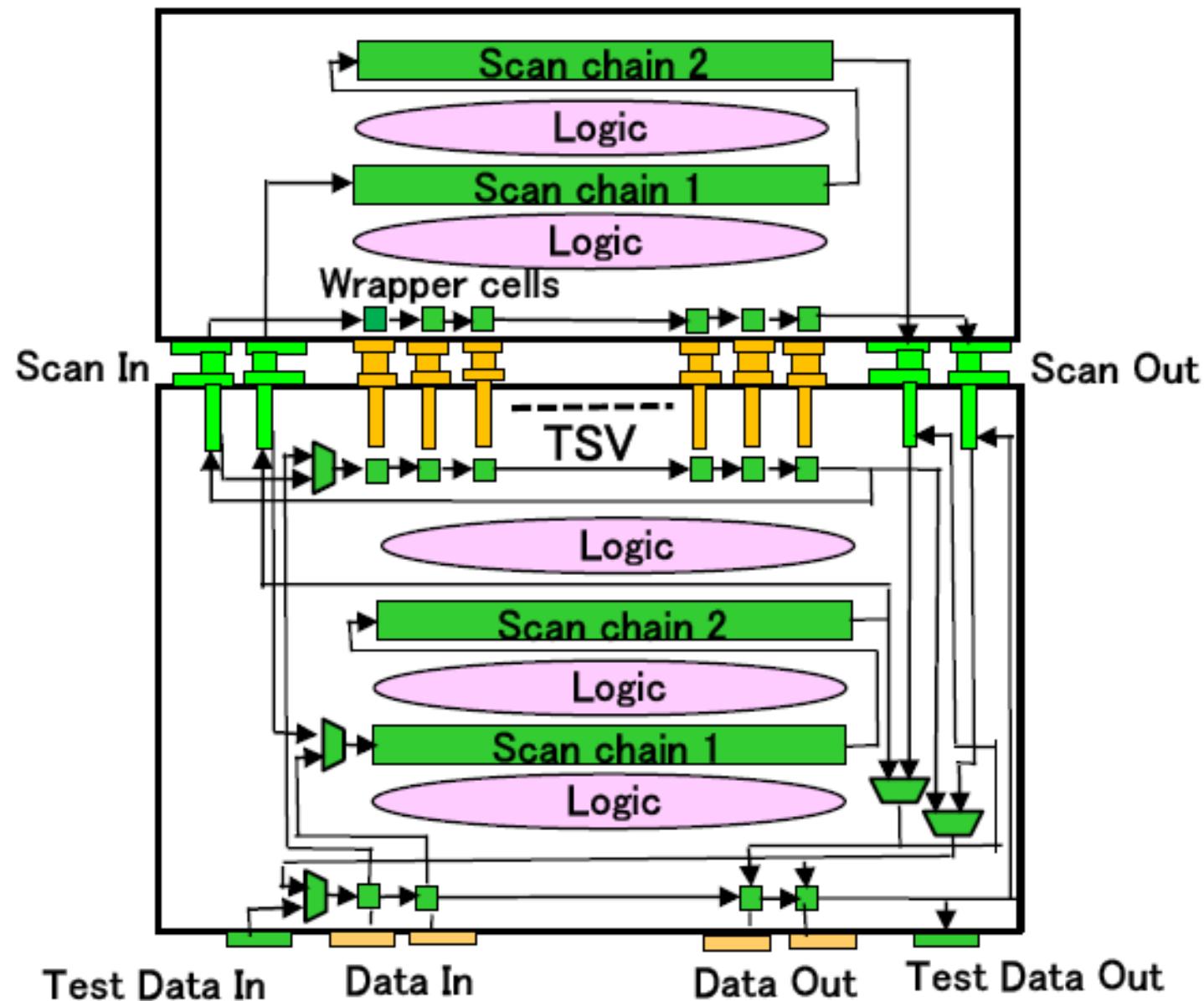
- **Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs**
- **Stack product: IEEE Std 1149.1**

3D-DfT Architecture

Test wrapper per die

- **Based on IEEE 1149.1 or 1500**
- **Two entry/exit points per die:**
 1. **Pre-bond : extra probe pads**
 2. **Post-bond: extra TSVs**

3次元 DFT アーキテクチャの検討



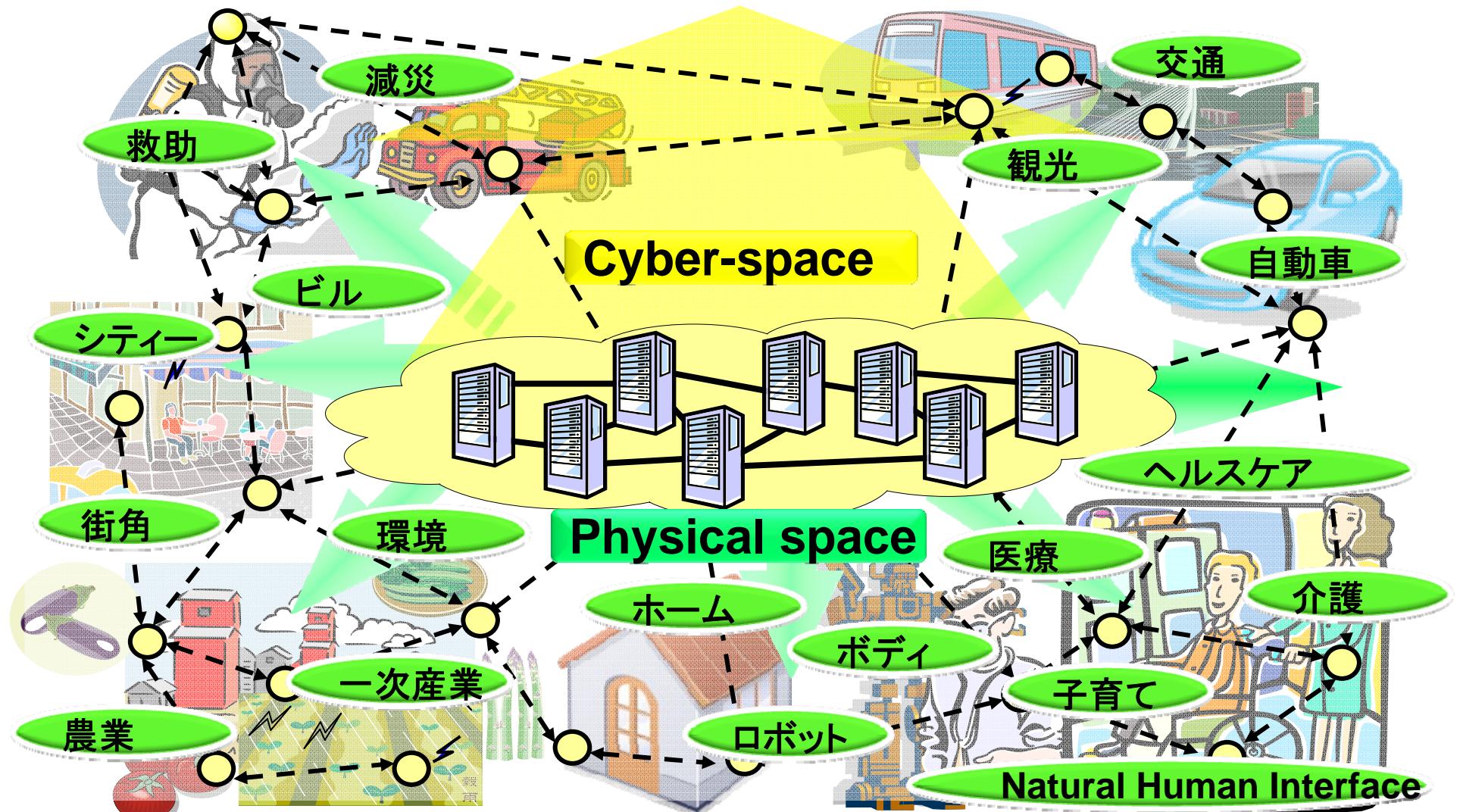
設計から見た 三次元積層技術の将来展望と課題

東京大学 教授 桜井貴康

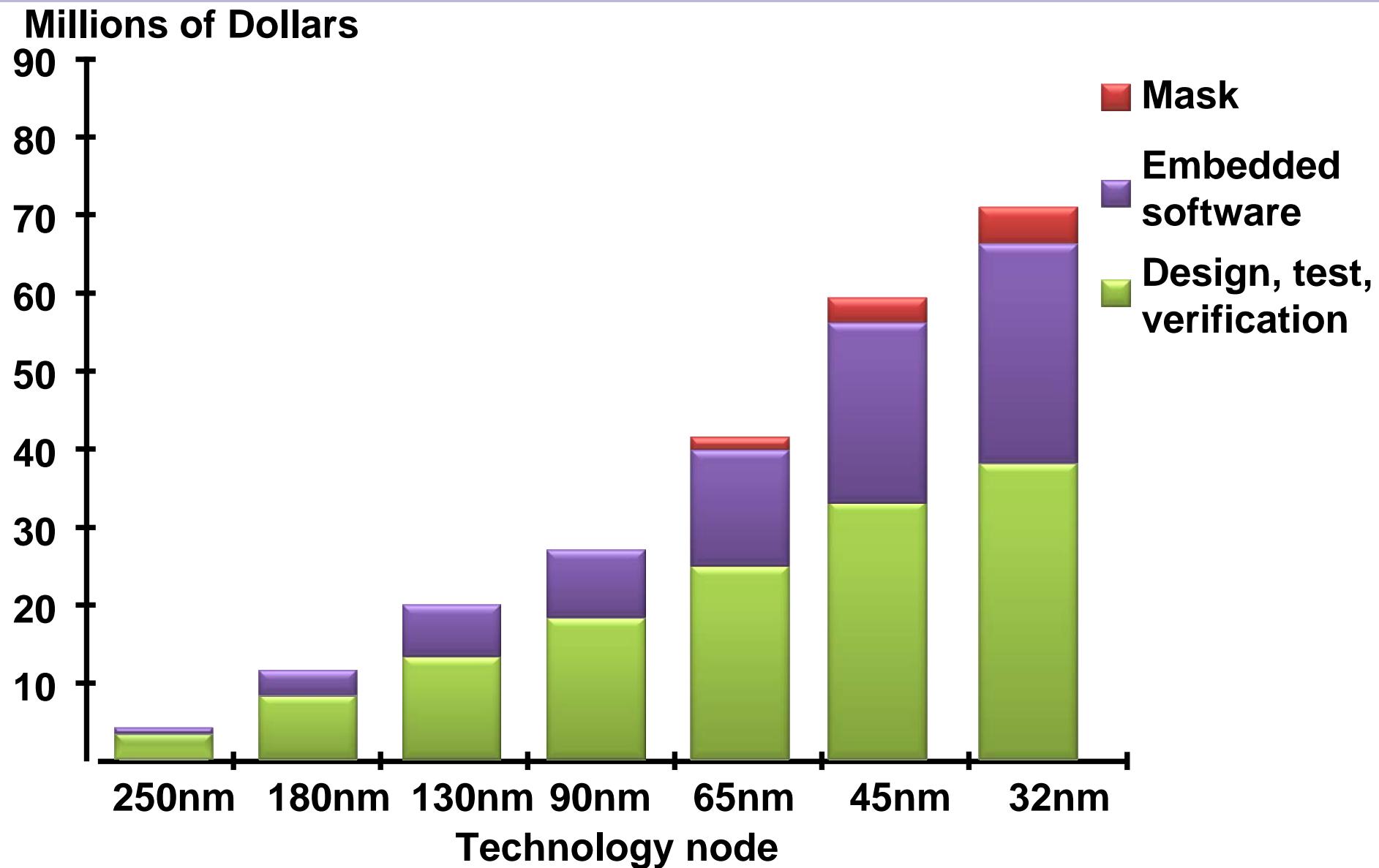
tsakurai@iis.u-tokyo.ac.jp

<http://lowpower.iis.u-tokyo.ac.jp/>

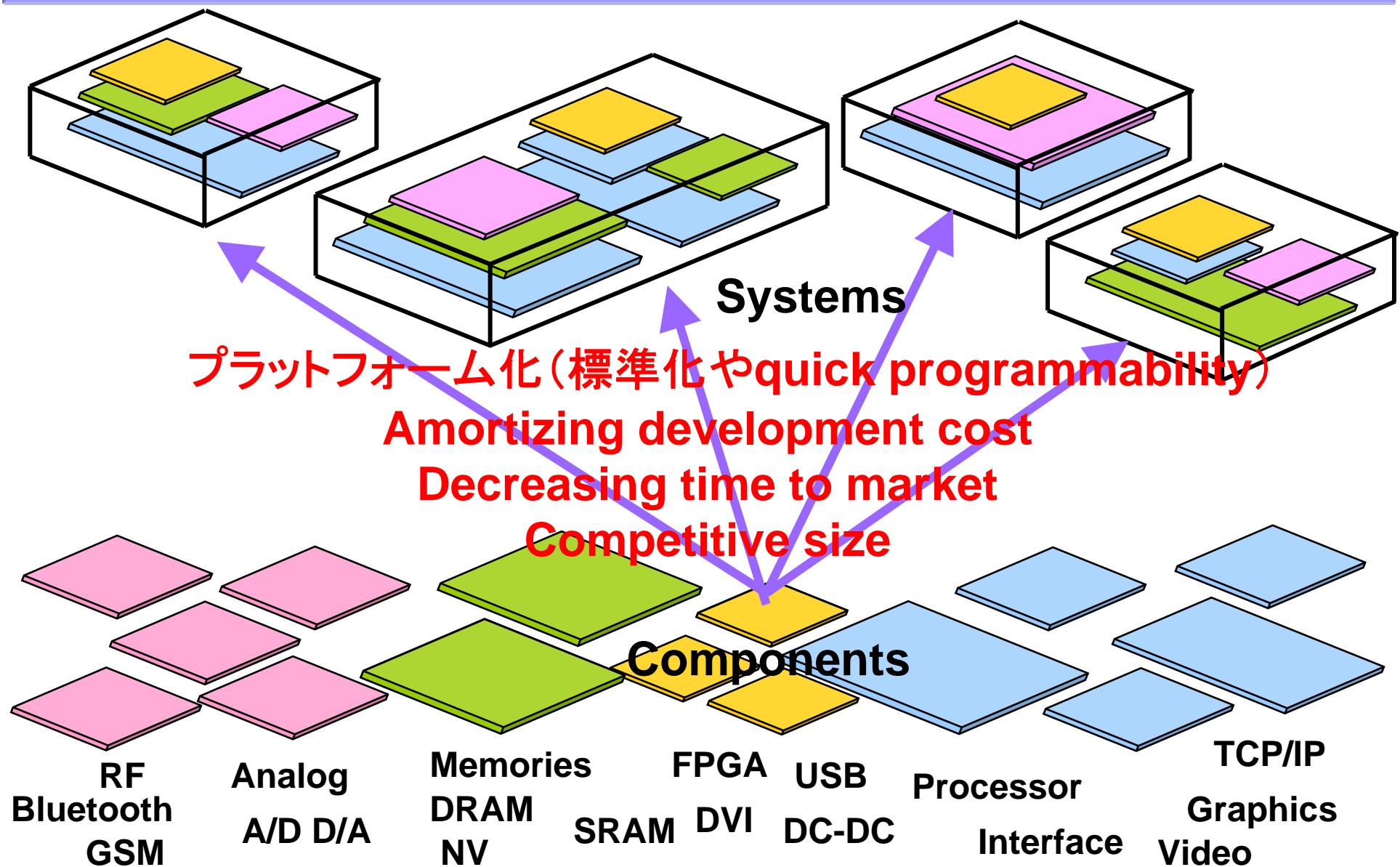
実空間をカバーし発展するIT社会インフラ



高騰する半導体集積回路の開発費

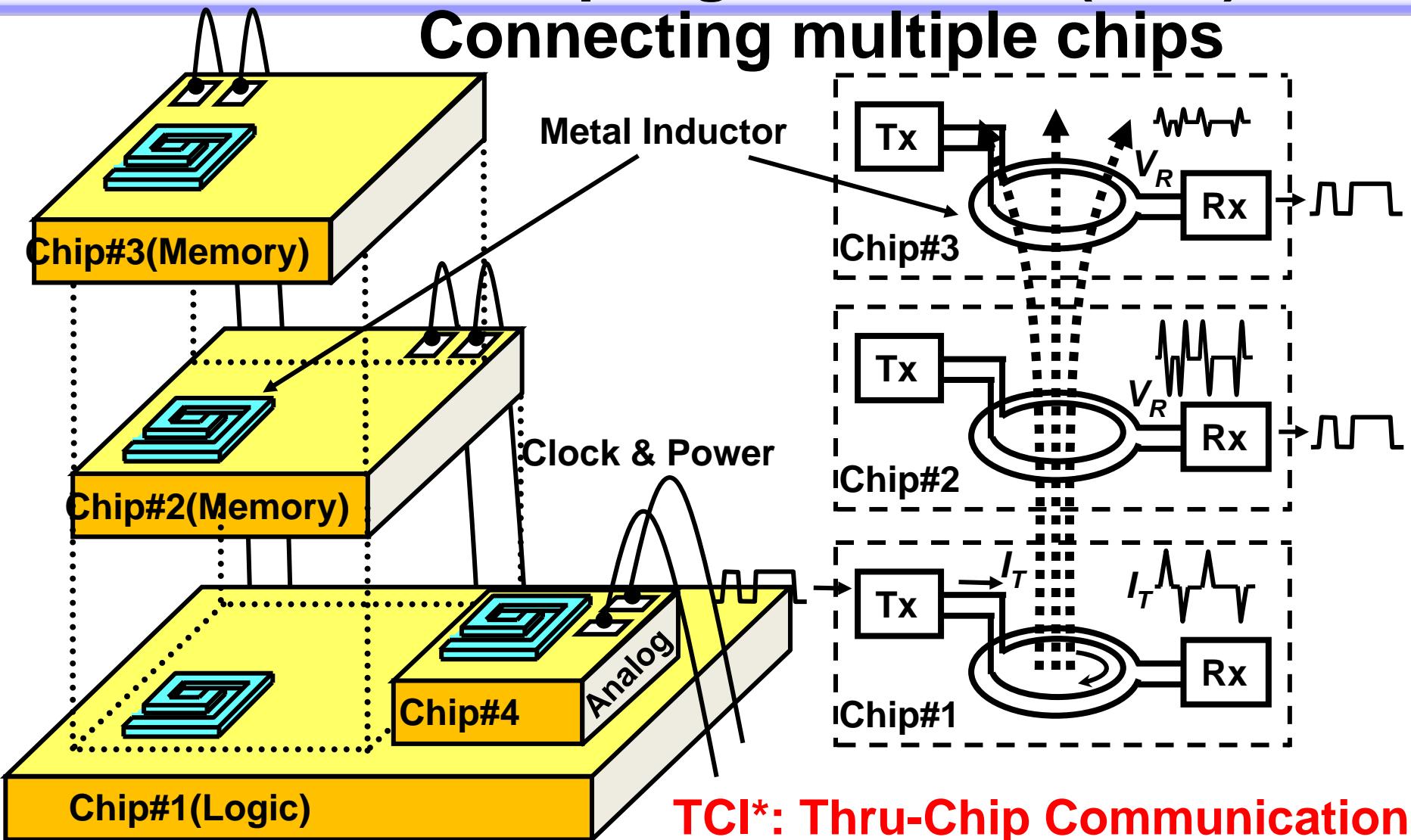


開発費・開発リスク・開発期間低減のための3D



Inductive-coupling interfaces (TCI*)

Connecting multiple chips

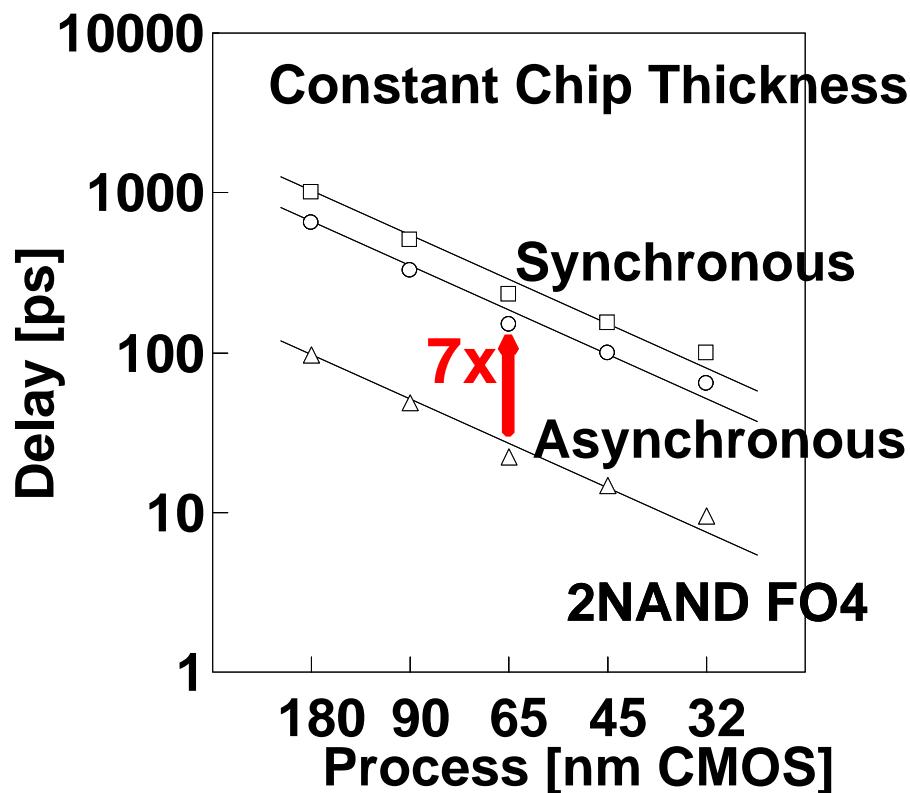


D. Mizoguchi, Y. Yusof, N. Miura, T. Sakurai, T. Kuroda, "A 1.2Gb/s/pin Wireless Superconnect based on Inductive Inter-chip Signaling (IIS)," ISSCC'04, pp. 142-143, Feb. 2004. N. Miura, D. Mizoguchi, Y. B. Yusof, T. Sakurai, and T. Kuroda, "Analysis and Design of Transceiver Circuit and Inductor Layout for Inductive Inter-chip Wireless Superconnect," Symp. on VLSI Circuits, pp. 246-249 June 2004.

T.Sakurai

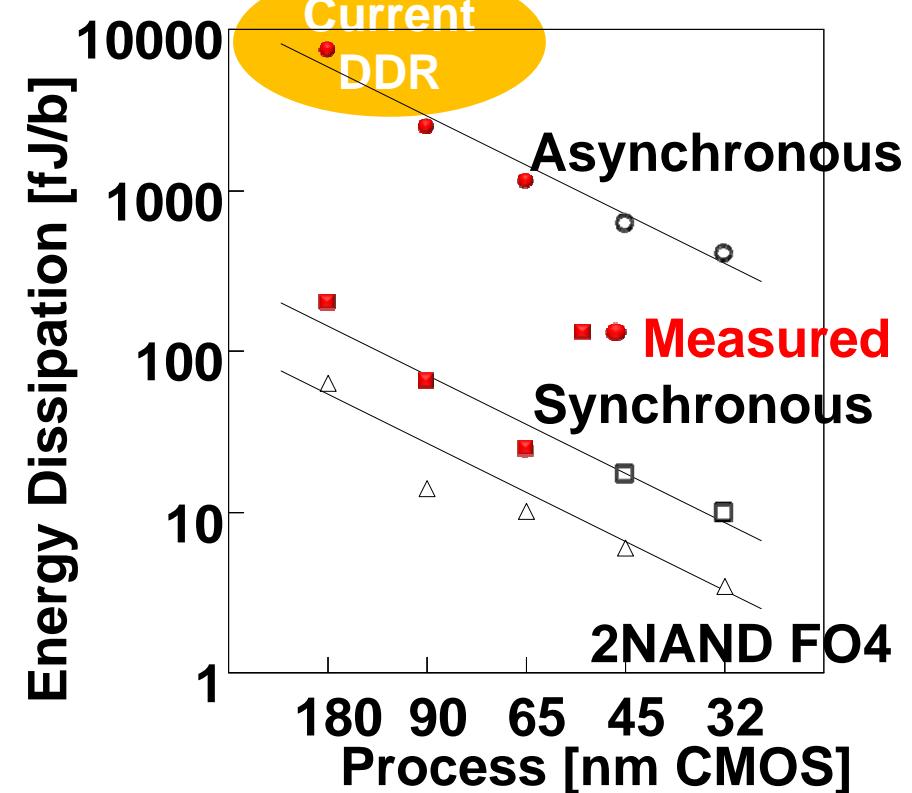
Performance scales

Delay



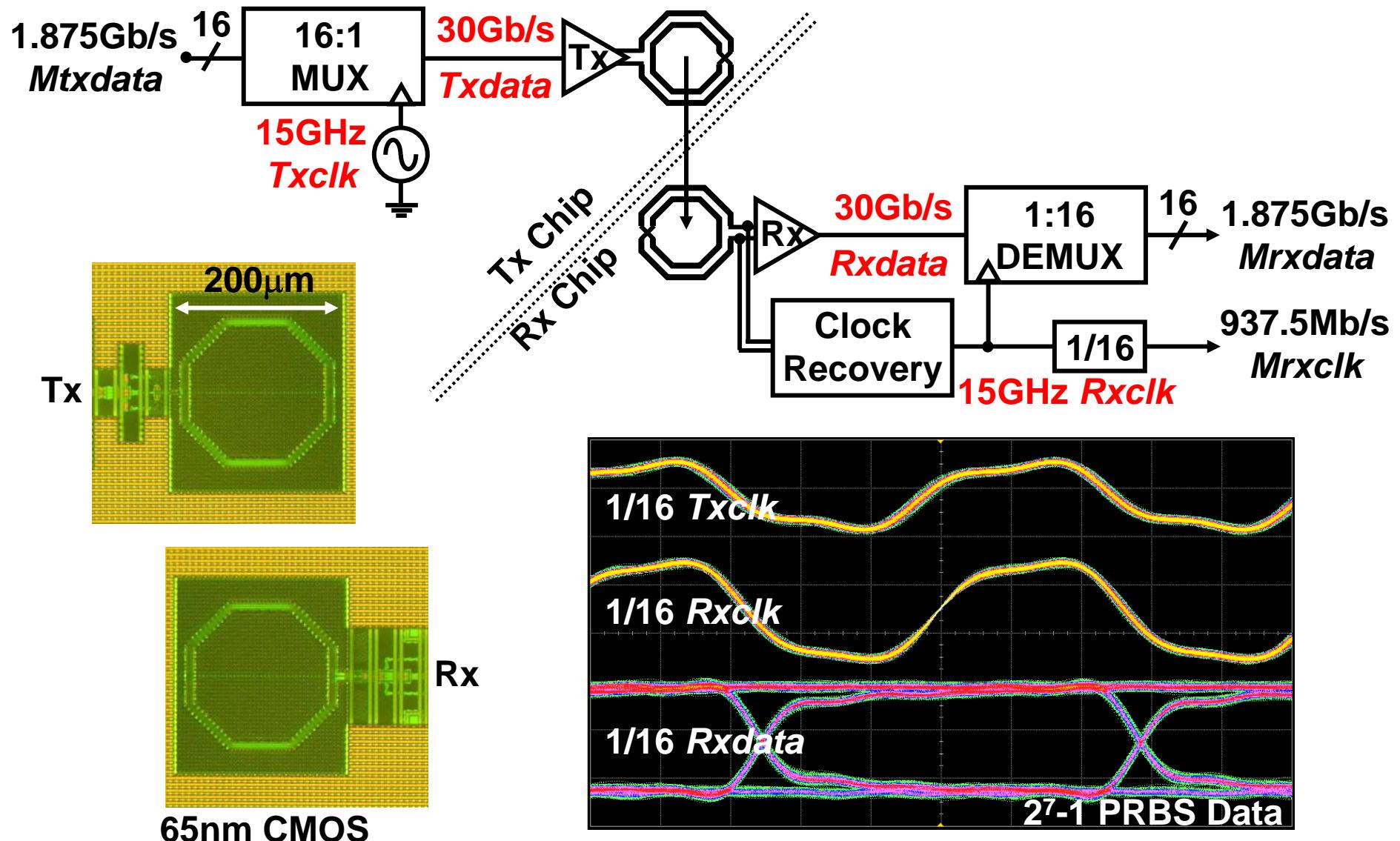
Delay is equivalent to 7 stages
of 2NAND FO4, or
0.5mm wire in 65nm.

Energy



Energy is equivalent to 4x
of 2NAND FO4.

30Gb/s/ch Clock and Data Transmission



Y.Take, N.Miura, T.Kuroda, "A 30Gb/s/link 2.2Tb/s/mm² Inductively-Coupled Injection-Locking CDR," A'SSSC'10, Nov. 2010.

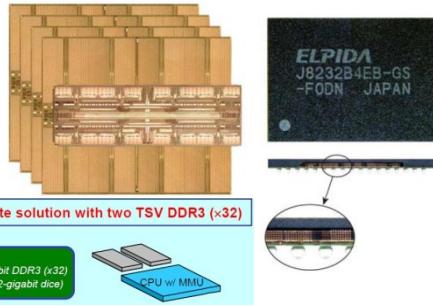
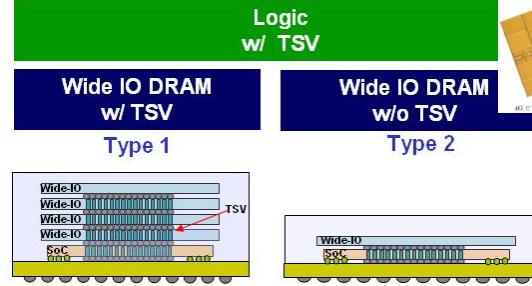
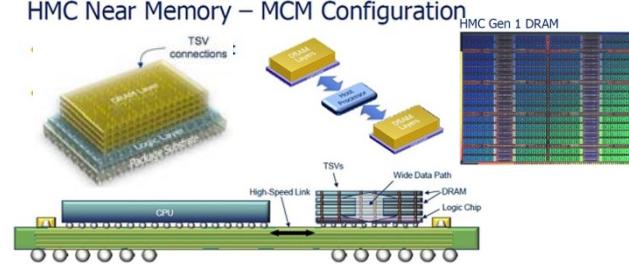
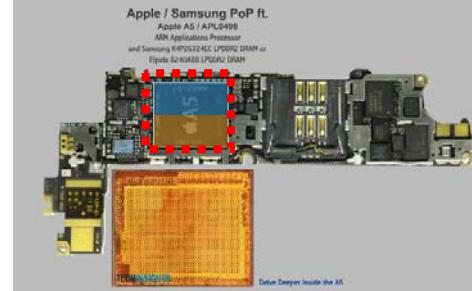
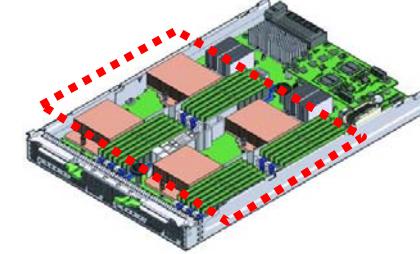
T.Sakurai

Challenges of Supply-Chain for 3D Stacking Systems

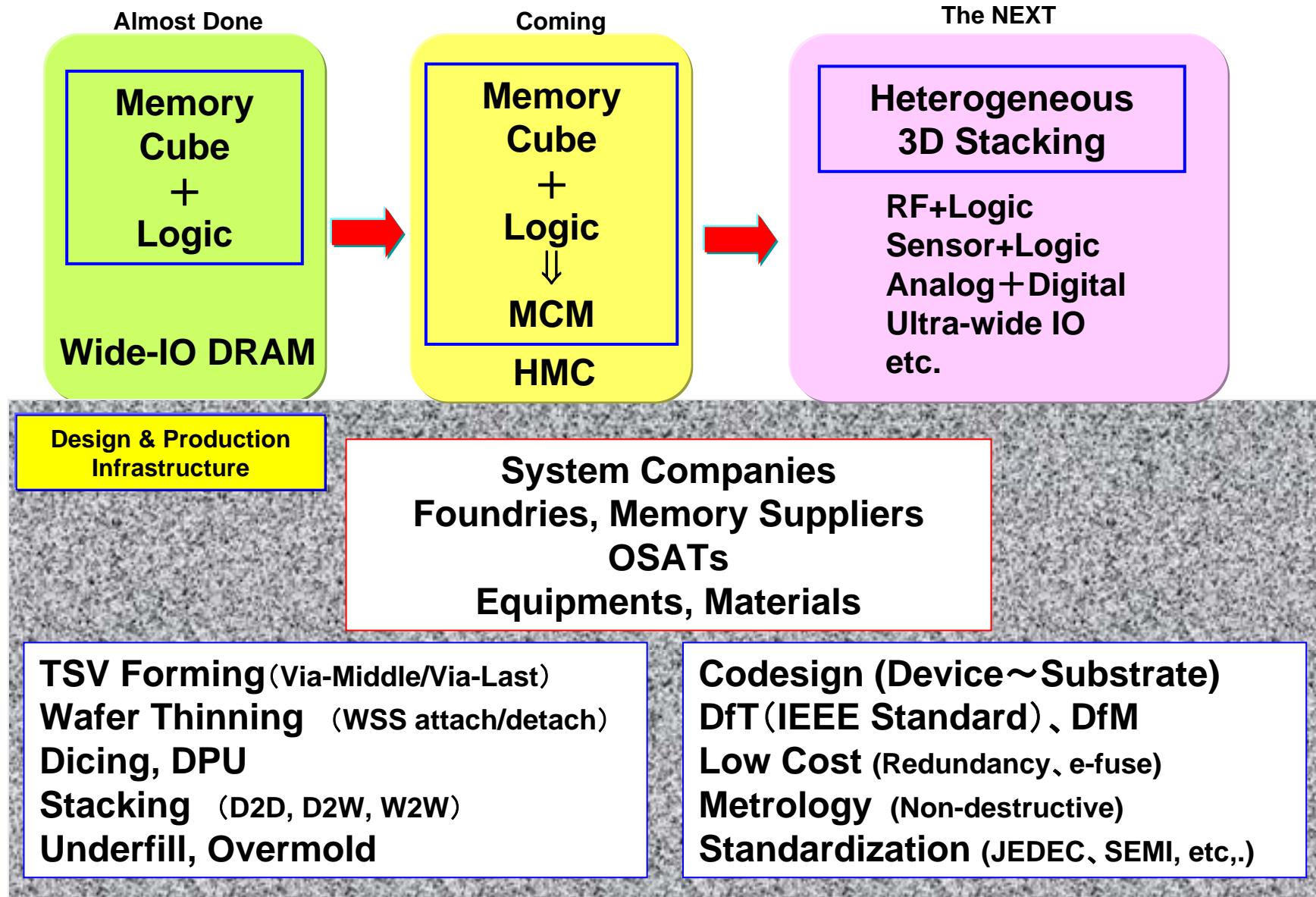
June, 2012

Hiroaki Ikeda
3D-Integration Technology Research Department,
ASET (Association of Super-Advanced Electronics Technologies)
[<http://www.aset.or.jp/>]

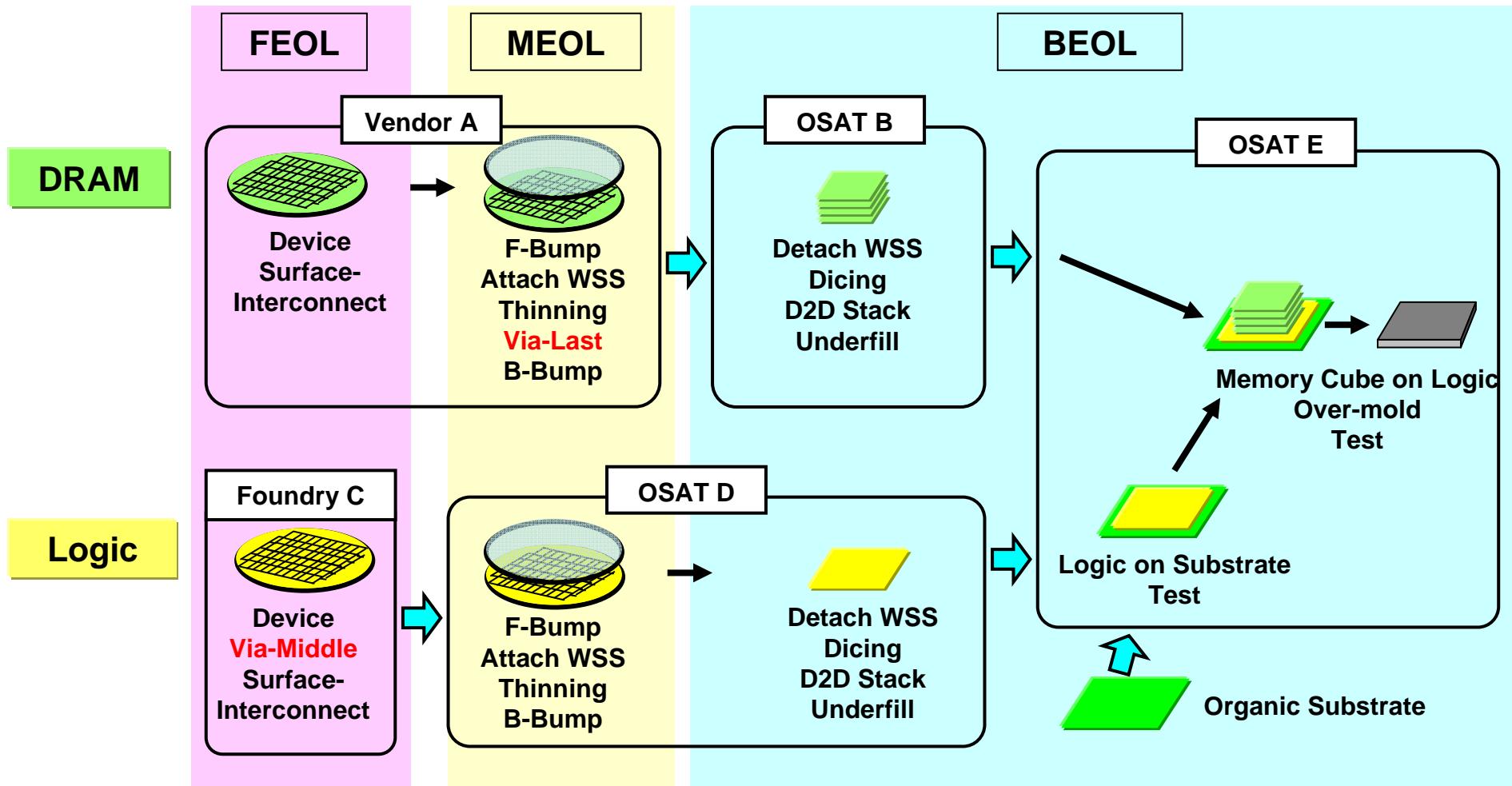
Predictable Application for 3D Stacked System

4-High Stack x32 DDR3 DRAM	1-4 High Stack Wide-IO(x512) DRAM	4-8 High Stack Hybrid Memory Cube
Small Footprint Low Power  <p>2-gigabyte solution with two TSV DDR3 (x32)</p> <p>2-gigabyte: Two 8-gigabit DDR3 (x32) (4 stacked 2-gigabit dice)</p> <p>CPU w/ MMU</p>	Low Power High Bandwidth 	High Bandwidth 
Thin Note PC  <p>Motherboard of Ultrabook</p>	Mobile Terminal  <p>Motherboard of Smart Phone</p>	Network Infra.  <p>Blade Server Unit</p>

Infrastructure for the next

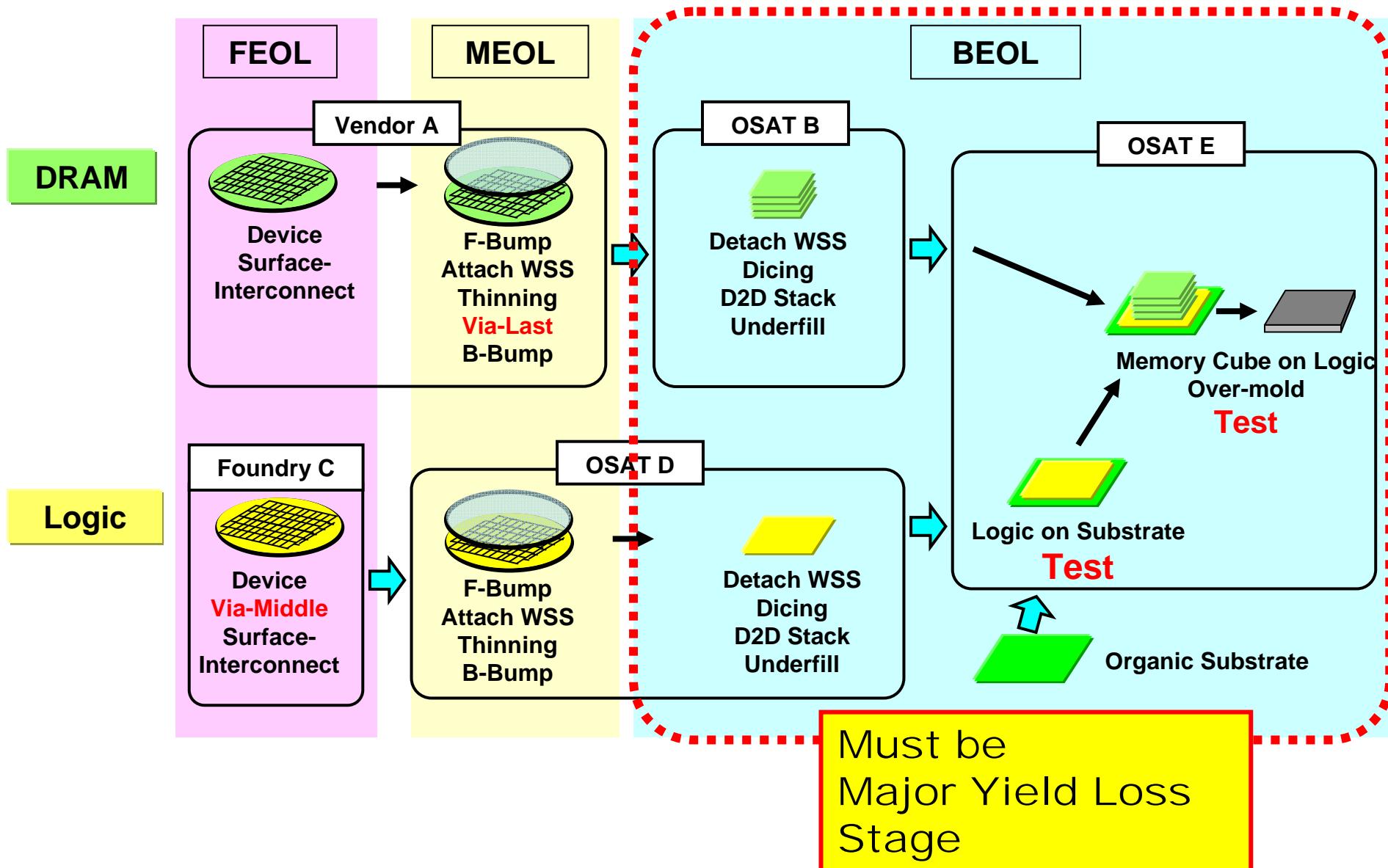


Supply Chain Example for Memory + Logic



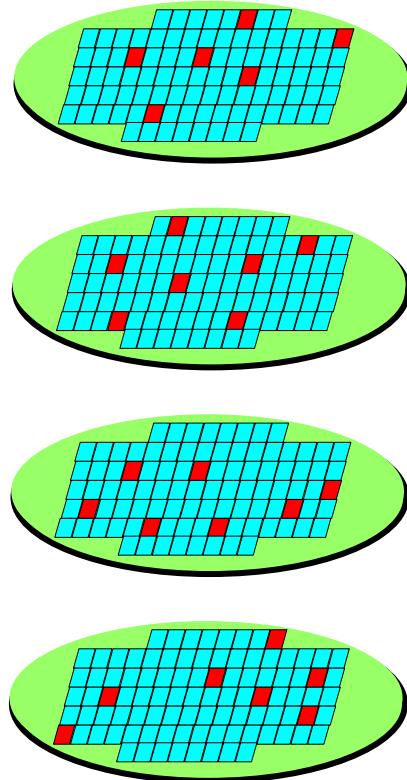
Memory Cubes will serve Supply Chains for Memory and Logic.
They are “Pipe-Cleaner” for volume production and more sophisticated devices.

Supply Chain Example for Memory + Logic

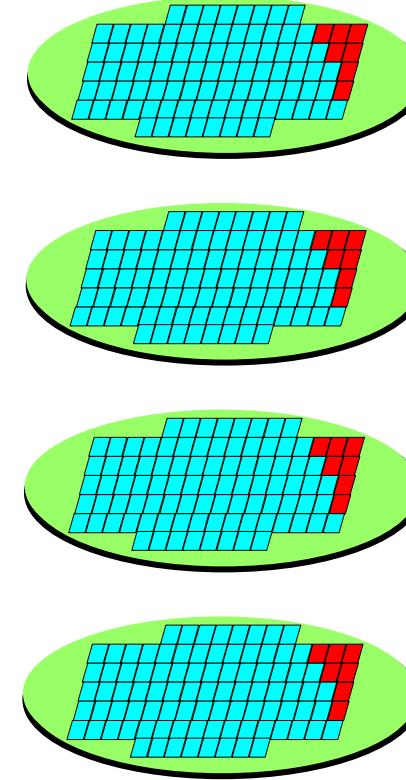


Homogeneous Stacking Yield (W2W)

Random Failures



Fixed Location Failures

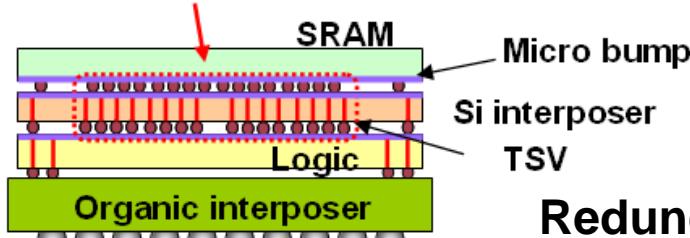


**Requires
better redundancy design
for random failures**

Underfill Solution?

Interconnects Failure Recovery

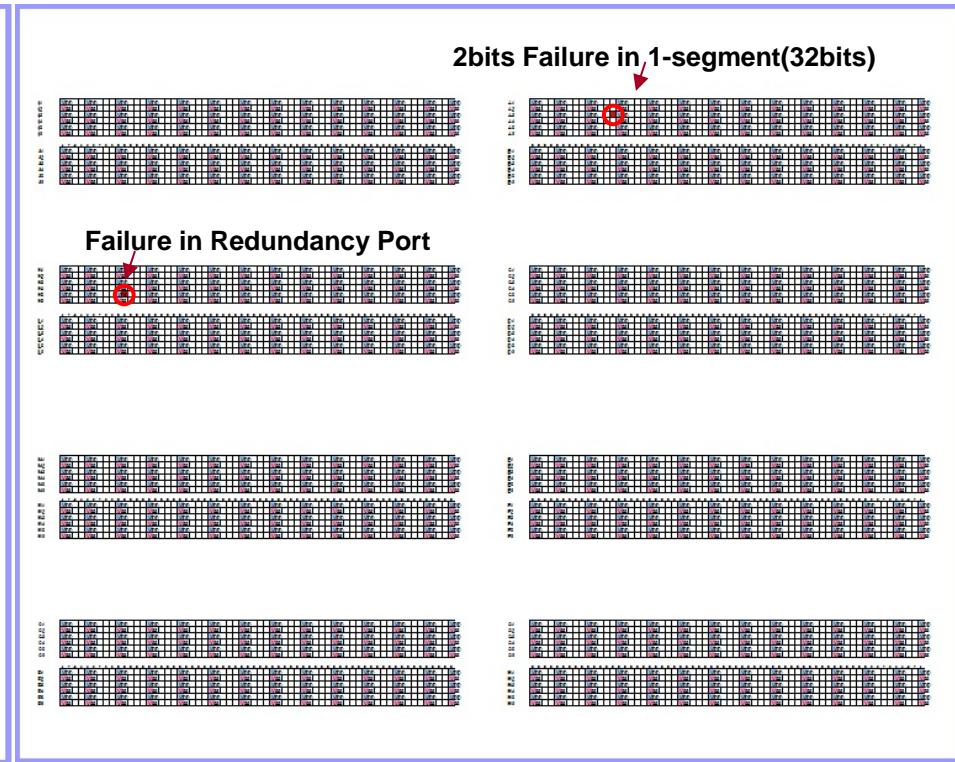
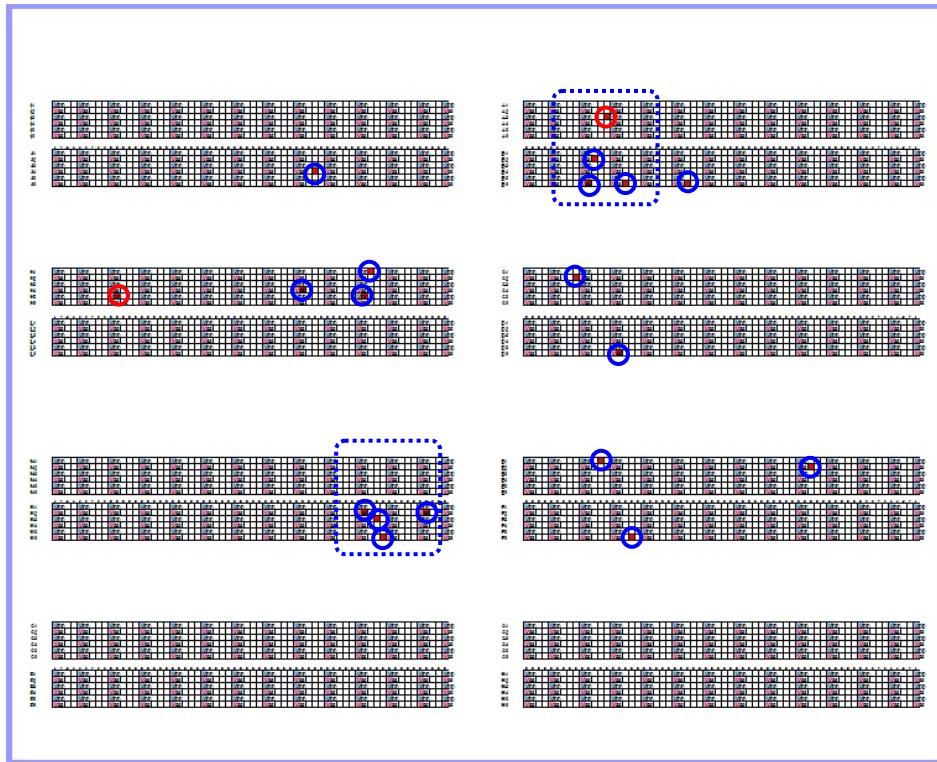
Ultra wide bus with 4,096 bumps



Redundancy
OFF
[18 failures]

1-TSV replace for every 32 TSVs' unit

Redundancy
ON
[2 failures]



Remaining Issues from Now

Lowering Cost:

- Lower TSV Forming Cost (Deep-Si Etch, Plating, etc)**
- Thinning without WSS**
- Faster Throughput of MEOL/BEOL**
- Dicing/DPU Yield Improvement**
- Stacking Yield Improvement**

Reliability:

- DfT** → BIST, SCAN, JTAG
- In-Situ Testing** → Direct probing to Micro-bumps
- Lowering Stress** → Countermeasure for Warpage
- Thermal Managements** → Cooling System Design

Advanced Failure Analysis:

- Non-destructive Metrologies (Physical/Electrical)**
- Co-design for DfT/DfM**