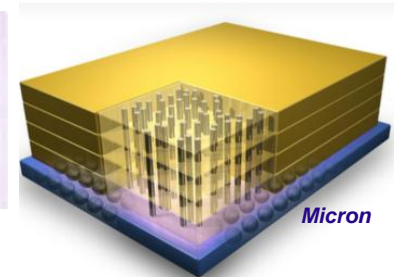
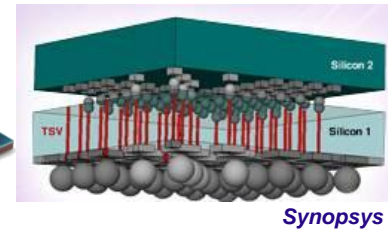
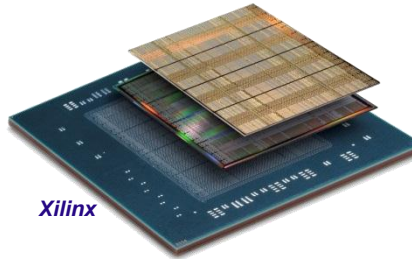
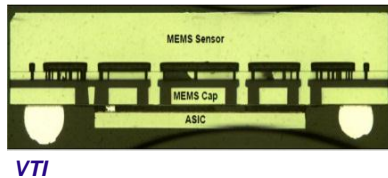
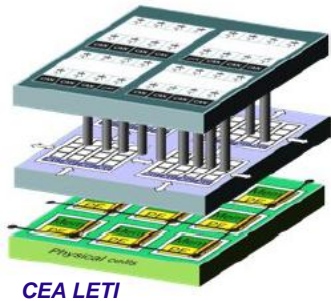


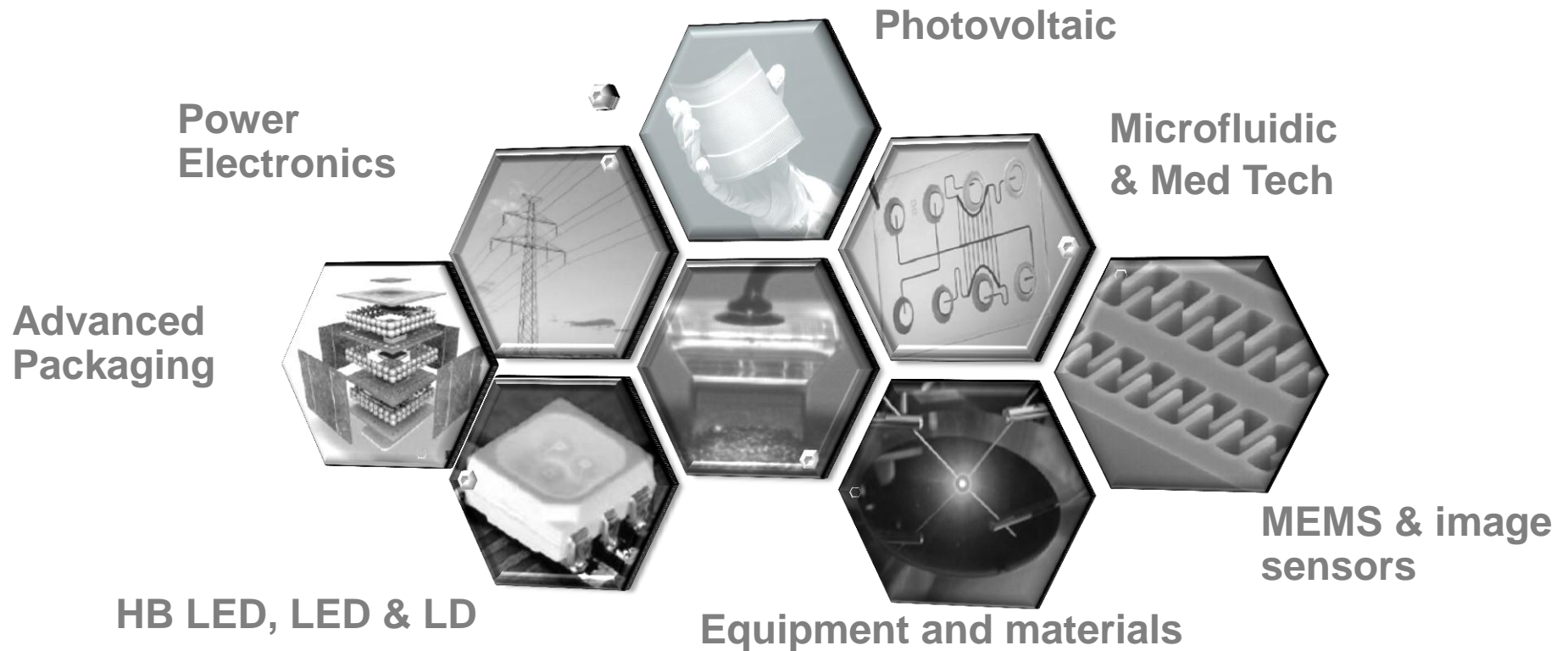
# 3DIC & TSV interconnects business update

ASET presentation.



# Fields of Expertise

- Yole Développement is a market, technology and strategy consulting company, founded in 1998. We operate in the following areas:



- Our expertise is based on research done by our in-house analysts, conducting open-ended interviews with most industry players.
  - 30 full time analysts with technical and marketing degrees
  - Primary research including over 3,500 interviews per year

# Mission Statement: Knowledge-Based Company

- **Help our customers develop their business through specific analysis, reports & services providing:**
  - **Accurate market data, market segmentation and marketing analysis**
  - **Technology evaluation; cost estimates and COO analysis**
  - **Patent portfolio analysis, licensing strategy and implementation**
  - **Identification of strategic development opportunities for companies and business units**
  - **Support for M&A, due diligence, and identifying new investors**
  - **Advertising opportunities in YOLE magazines, webcasts and specific events**
- **You get operational results from Yole analysis and actions**

# 4 Business Models

- **Custom Analysis:**

- Largest part of Yole activities
- Covered by NDA agreement
- A few days to several months of work, depending on objectives

- **Published Reports:**

- An average of 40 reports published every year
- Available individually or through Annual Subscription Program
- Market and technology reports, Patent analysis, Reverse Engineering/Costing reports and Reverse Costing tools

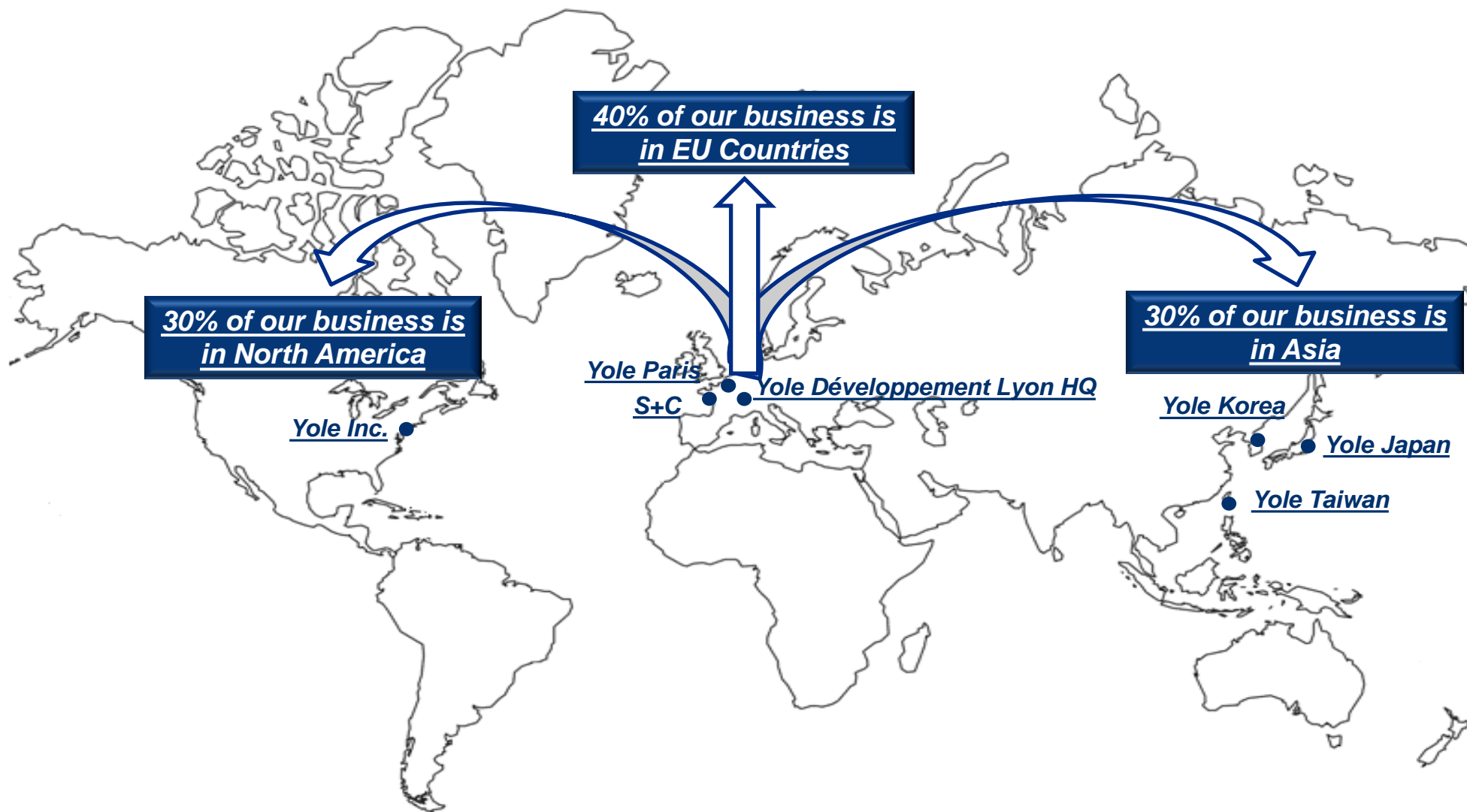
- **i-Micronews Media:**

- Newsletters and webcasts on 3D, MEMS, Power electronics, LED and imaging
- Advertising services providing access to our 45 000+ subscribers to be visible and diffuse information on your company and products

- **Yole Finance services:**

- M&A (buying and selling)
- Due diligence
- Fund-raising services

# Our Global Activity



# Some of Our Customers

## Financial investors & industry advocates



## R&D Organizations



## Suppliers (equipment, wafers, materials)



## Component manufacturers

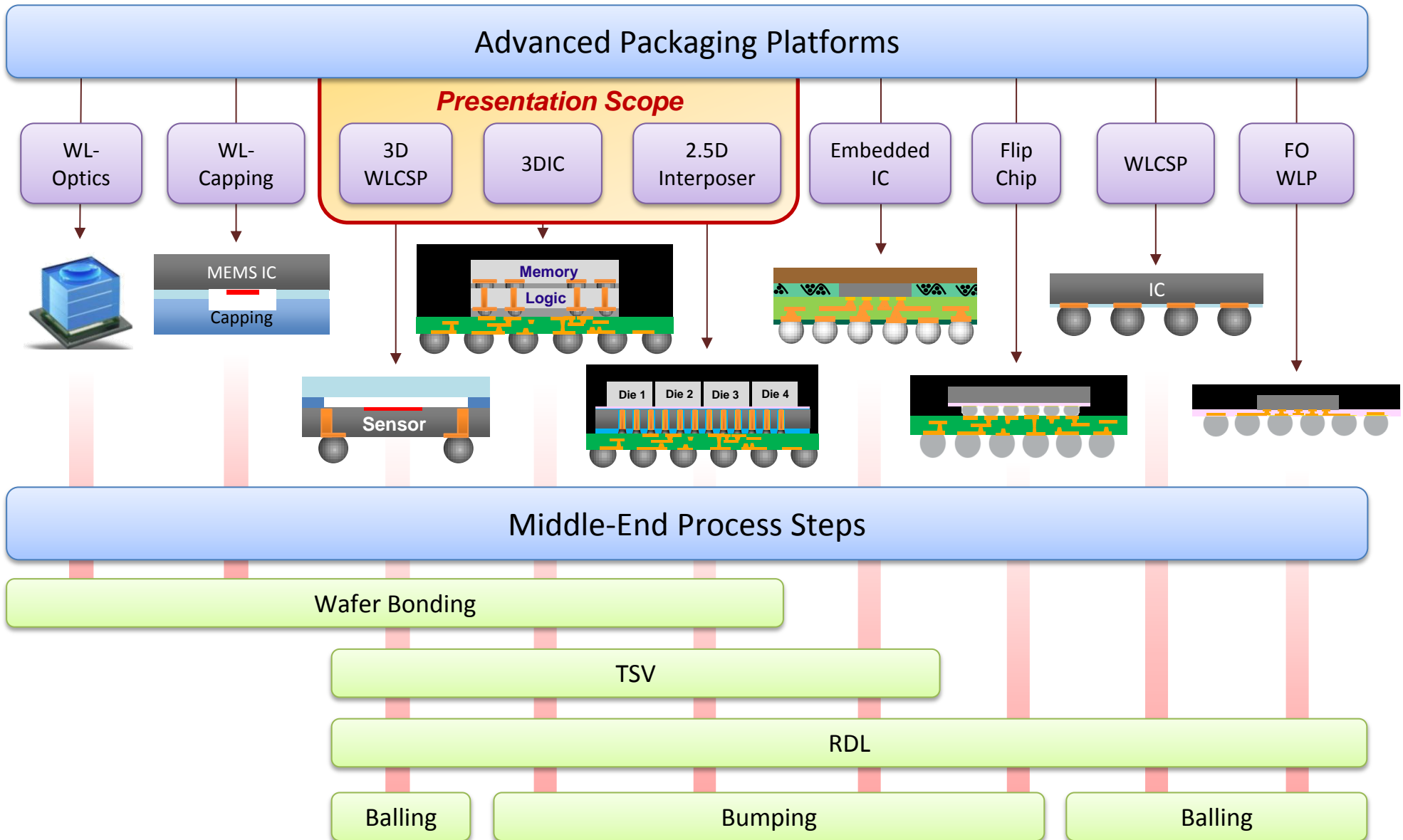


## Integrators, system suppliers & end users

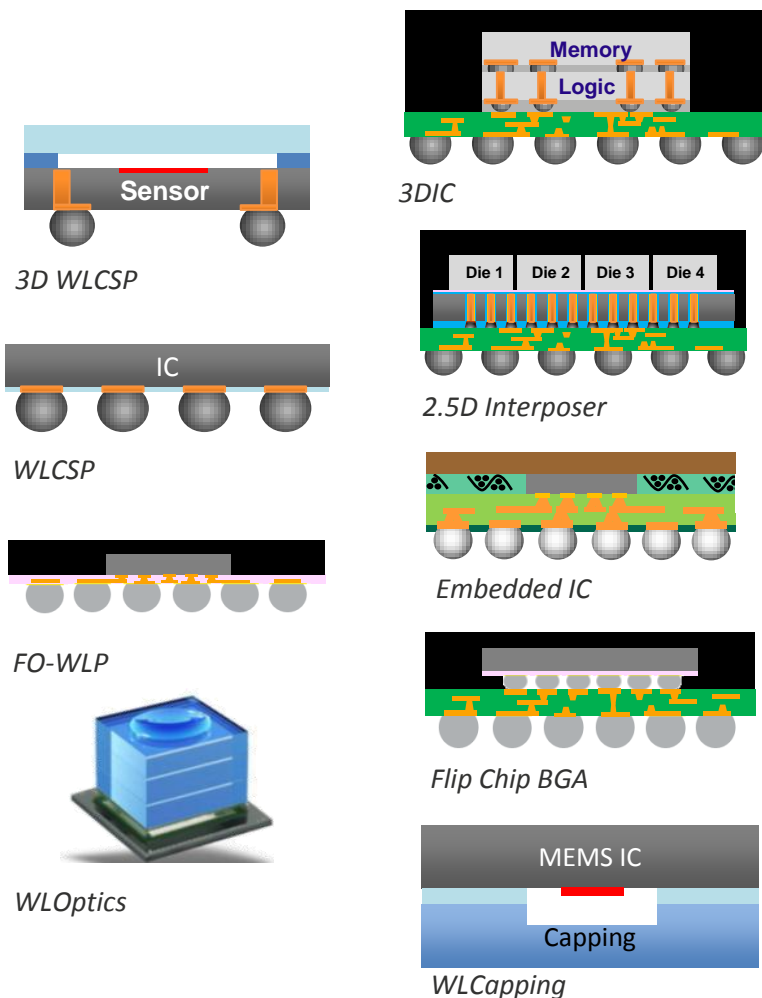




# Presentation Scope



# Packaging Platforms Studied Through Top-Down Approach



AP Platforms	Device type		Mid-end Process Steps				
	Active	Passive	Wafer Bonding	TSV	RDL	Bumping	Balling
3D IC	X		Optional	X	Optional	Optional (μ-bump)	
3D WLCSP	X		X	X	X		X
2.5D Interposers		X		X	X	Double Side	
WLCSP	X	X			X		X
Embedded Die	X	X			X	X	
FOWLP	X	X			X		X
Flip-Chip	X				Optional	X	
WLOptics		X	X				
WLCapping	X	X	X				

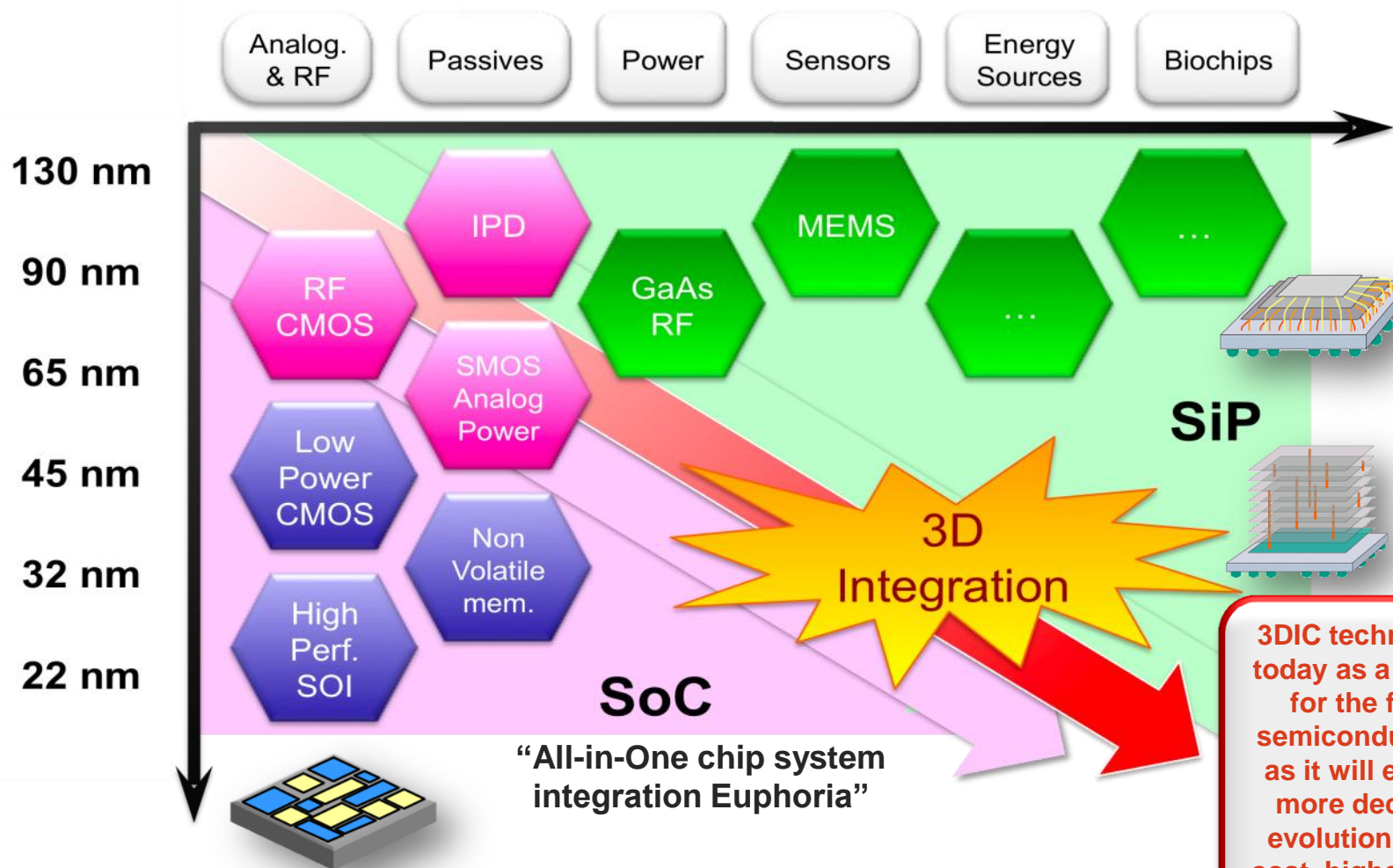
- For each of the studied device packaging possibilities is considered and modeled with a penetration rate
- Knowing the IC forecast (in unit and wafer), advanced packaging forecasts are extracted
- In this report, three advanced packaging platforms are considered: 3DIC, 3D WLCSP and 2.5D Interposer



# 3D Integration: Halfway Between SoC and SiP

## More Than Moore : diversification

More Moore : miniaturization



3DIC technology is seen today as a new paradigm for the future of the semiconductor industry, as it will enable several more decades of chip evolution at ever lower cost, higher performance and smaller-size features.

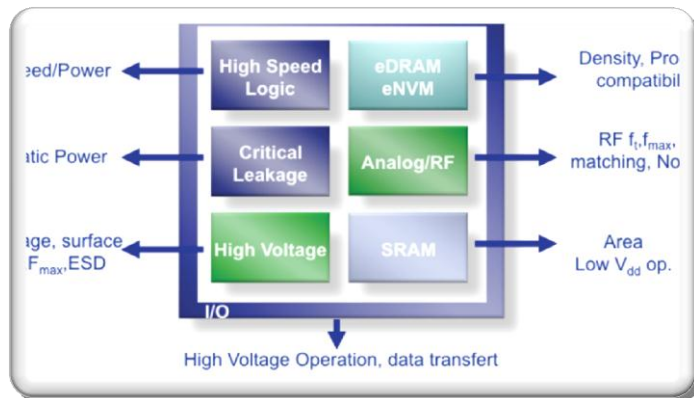
# Why, When and How 3D?

The rapid evolution of 3D thinking in the IC community is astonishing

- Two years ago, the big question was “Why 3D?”
- Today’s questions are “When 3D?” and “How 3D?”
- In less than a decade from now, we will wonder “Why 2D?”

## 2D SOC

“All-in-One chip system integration”



All functions on 28nm lithography

→ Chip area ↑, Cost ↑

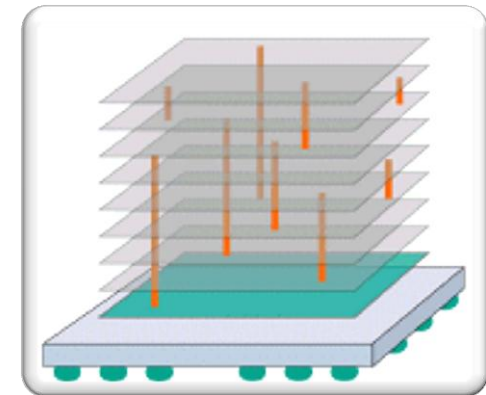


Thanks to 3D, heterogeneous functions are integrated:

- On different lithography nodes
- On different wafer sizes
- In different wafer fabs
- By different players

## 3DIC / 3D SoC

“De-integrated & Re-integrated SOC”

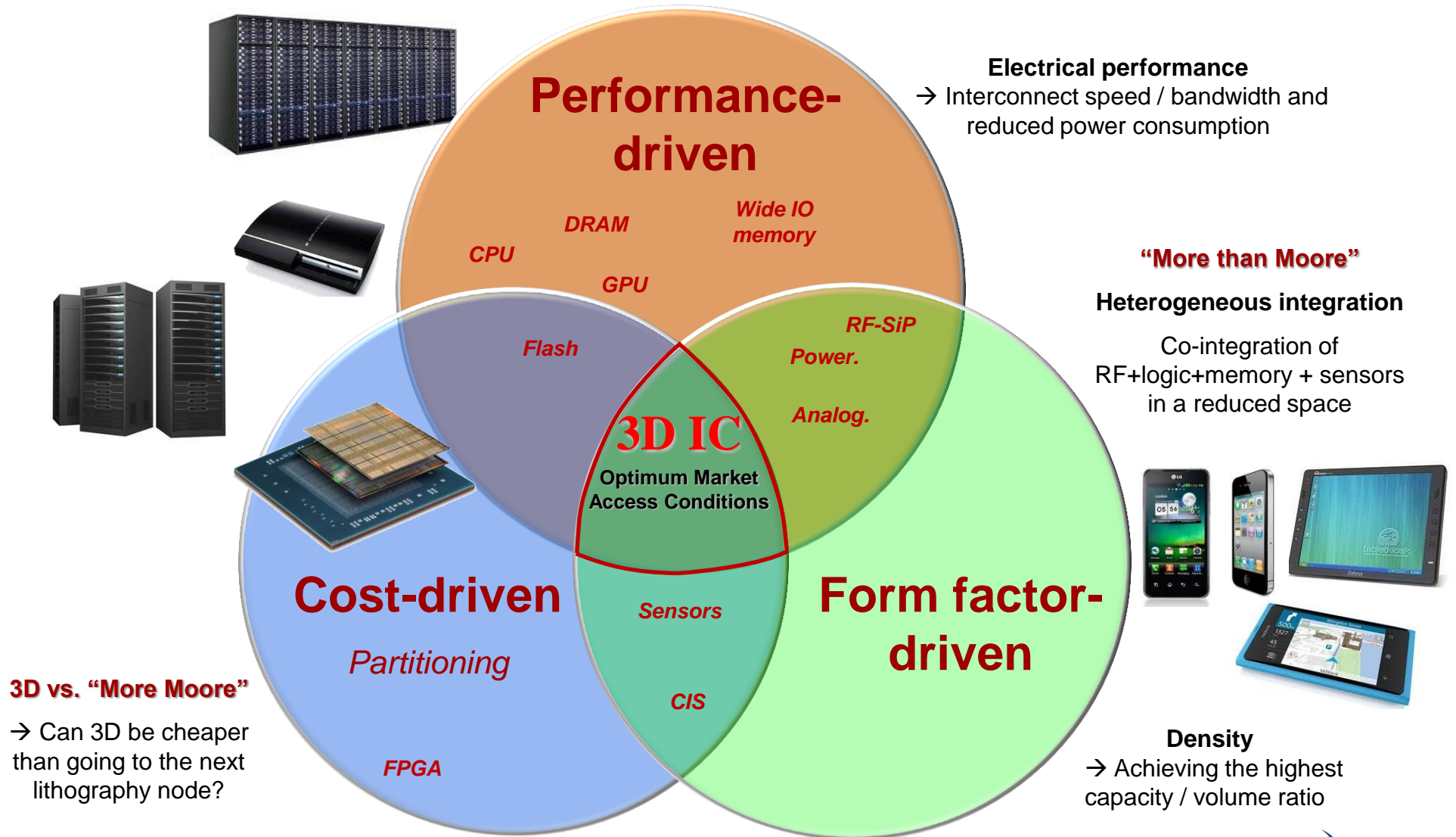


<b>MEMS</b>	130 nm	200 mm
<b>Memory</b>	45 nm	300 mm
<b>Logic</b>	22 nm ?	450 mm ?
<b>Analog</b>	90 nm	300 mm

→ Cost ↓, Performance ↑, Size ↓

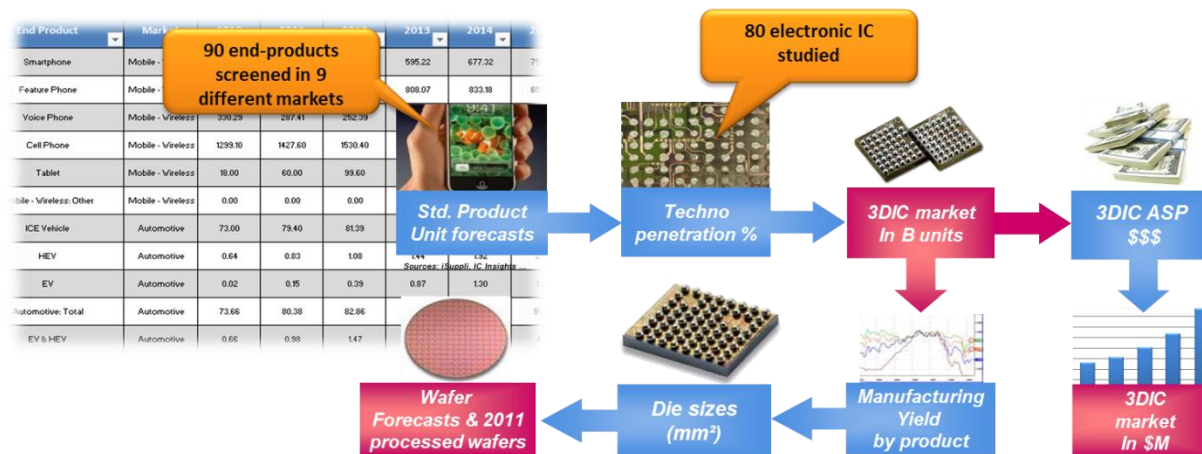
# 3D IC Market Drivers

*Unchanged since 2010!*



# 3DIC & TSV Market Forecast

## Top-Down Analysis

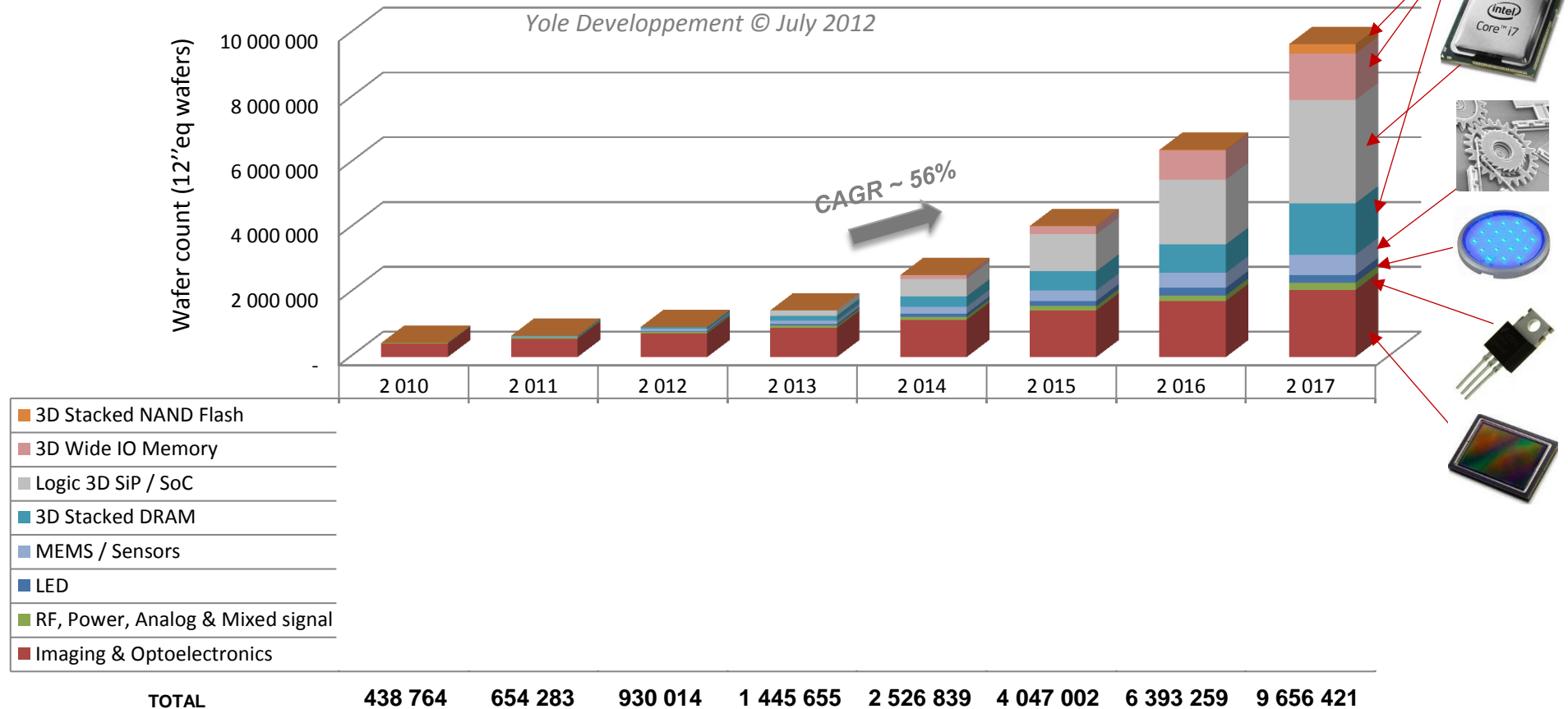


# Global TSV Chip Wafer Forecast

Breakdown by segment (12"eq. wafers)

## Global TSV Chip Wafer Forecast (All 3D Platforms)

Breakdown by Segment (12"eq wafers)



- Logic 3D SoC/SiP (including interposer chips, APE, CPU, FPGA, wide IO memory, etc.) is poised to become the most important industry using 3D platforms over the next few years

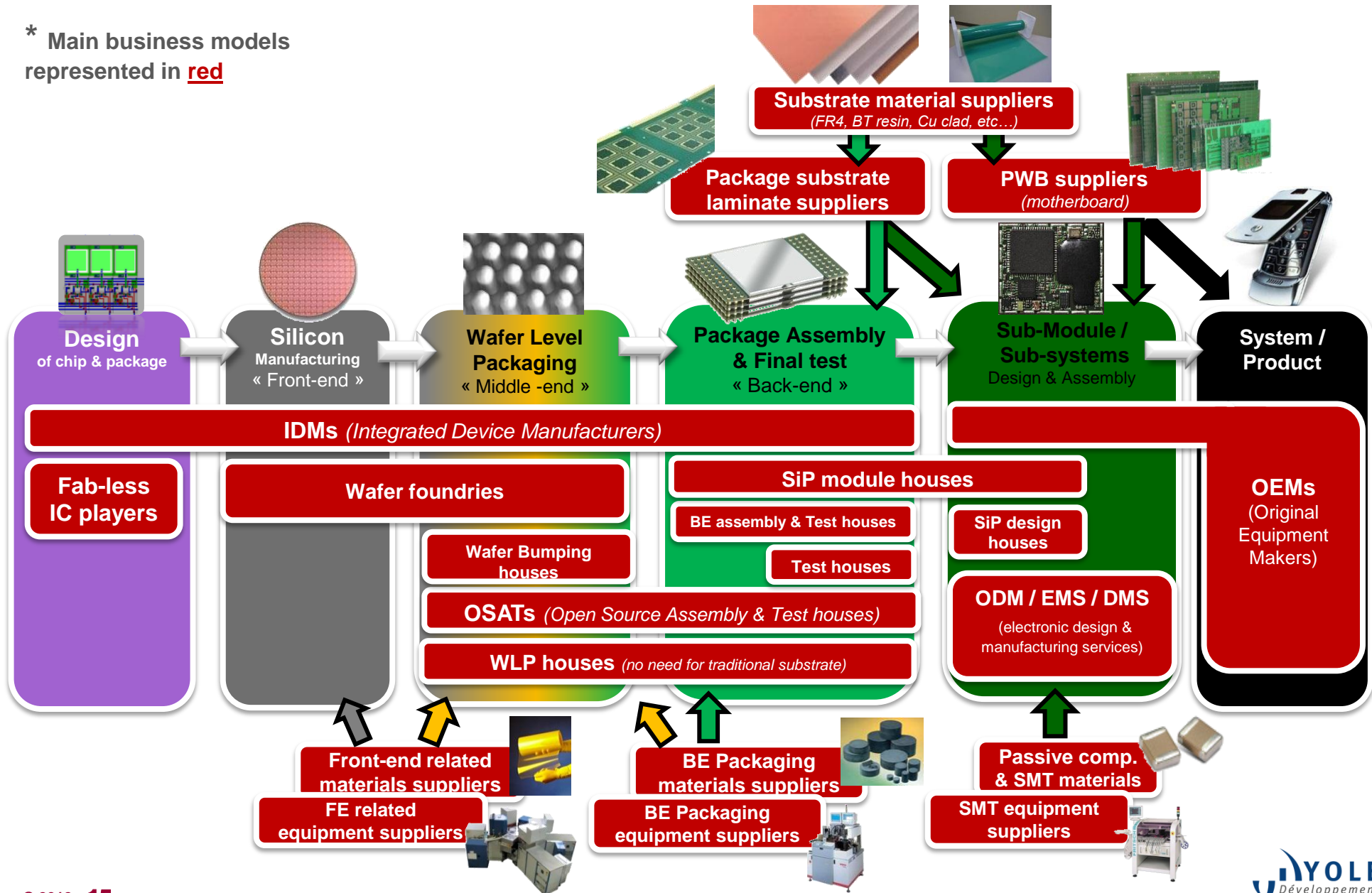
# Infrastructure & Supply Chain Analysis





# Traditional IC Packaging Supply Chain\*

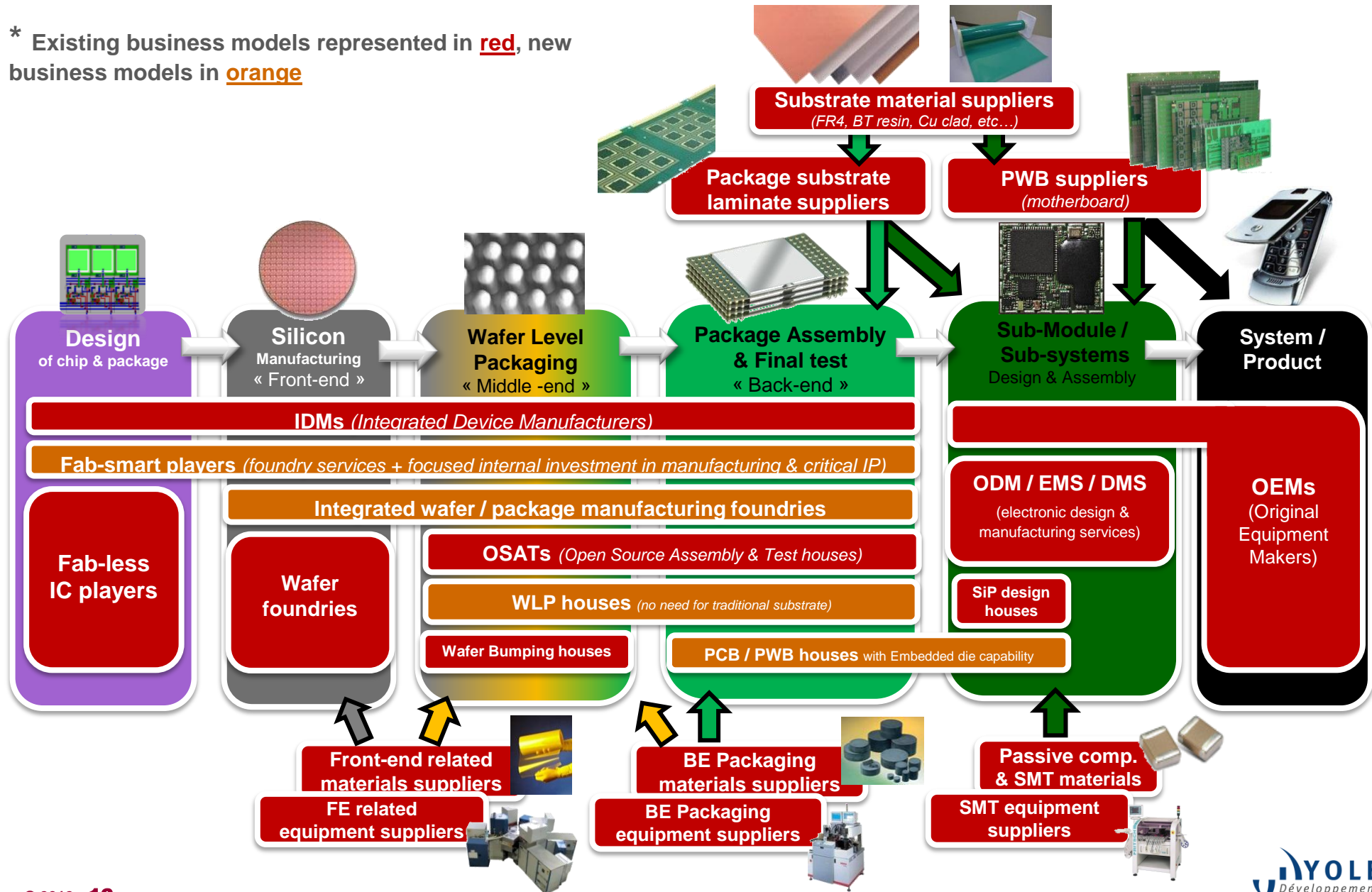
\* Main business models represented in **red**





# Transforming IC Packaging Supply Chain\*

\* Existing business models represented in **red**, new business models in **orange**



**SHARP.**

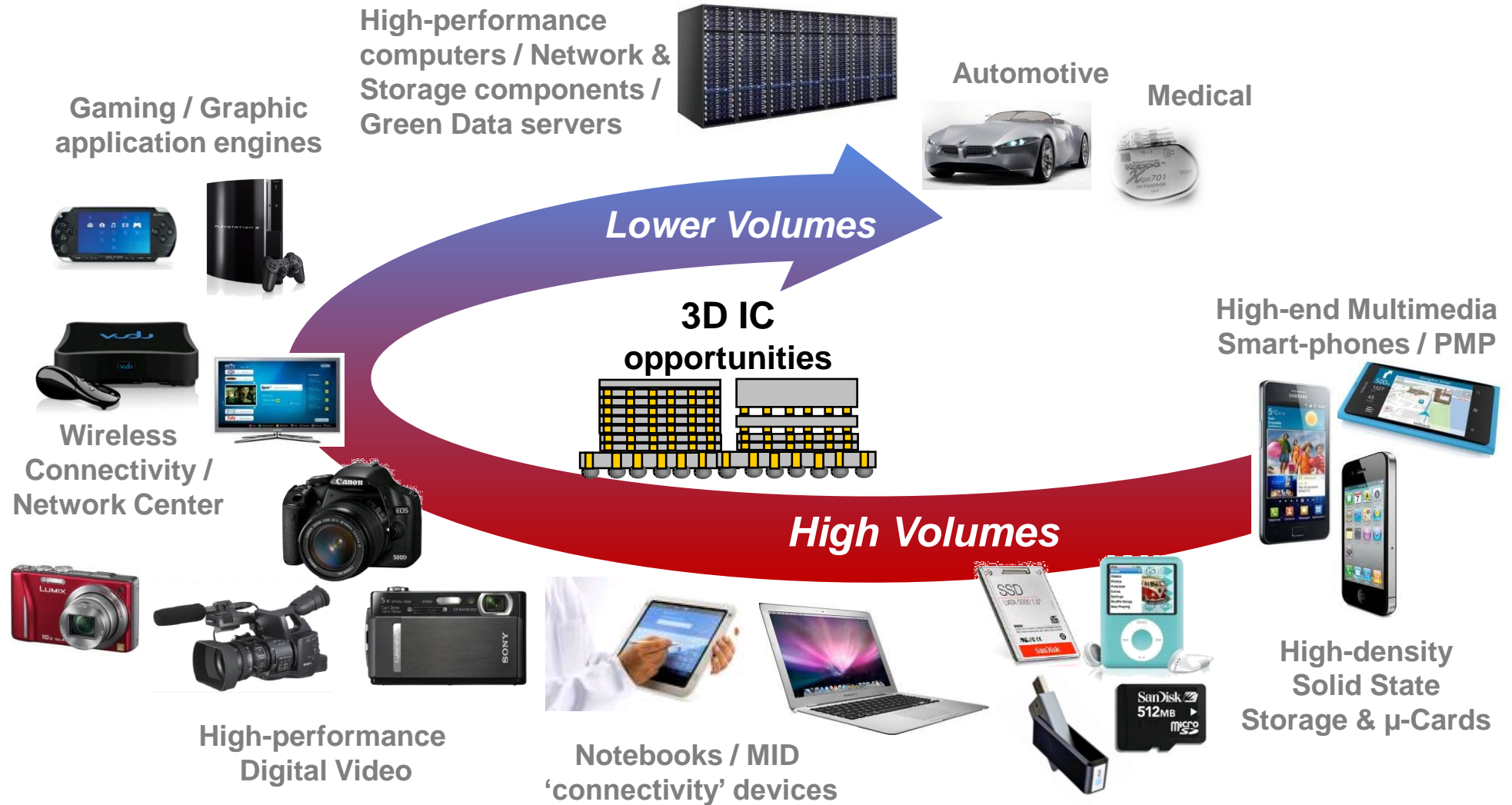


# 3D IC & TSV Market Focus





# What are the Markets for 3D ICs?



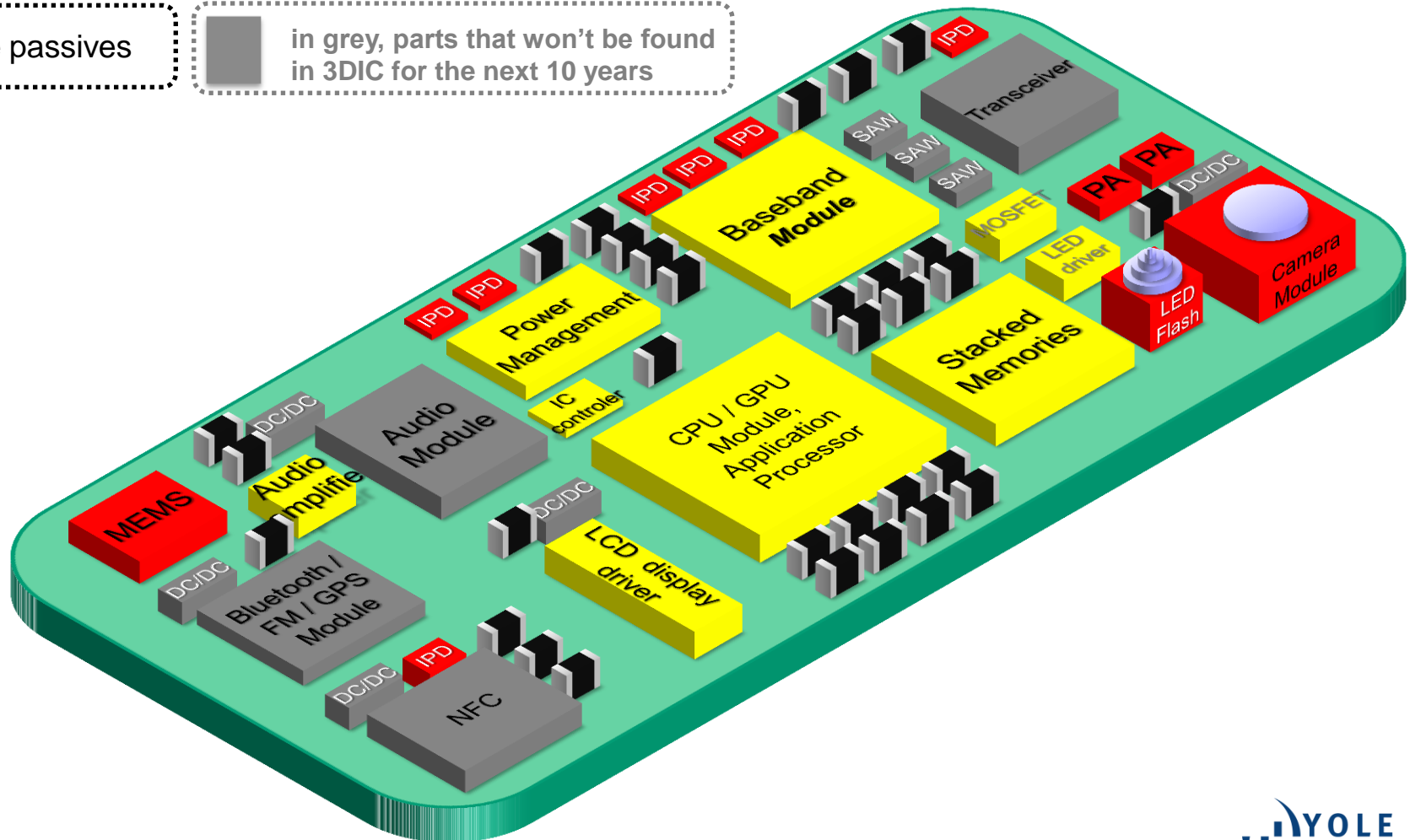
- 3D integrated ICs will be introduced in a variety of applications, all with their own specifications, challenges and individual roadmaps!

**in orange: these devices can be currently found with 3D TSV**

in yellow, parts which can be found in 3DIC's future

## Discrete passives

in grey, parts that won't be found  
in 3DIC for the next 10 years



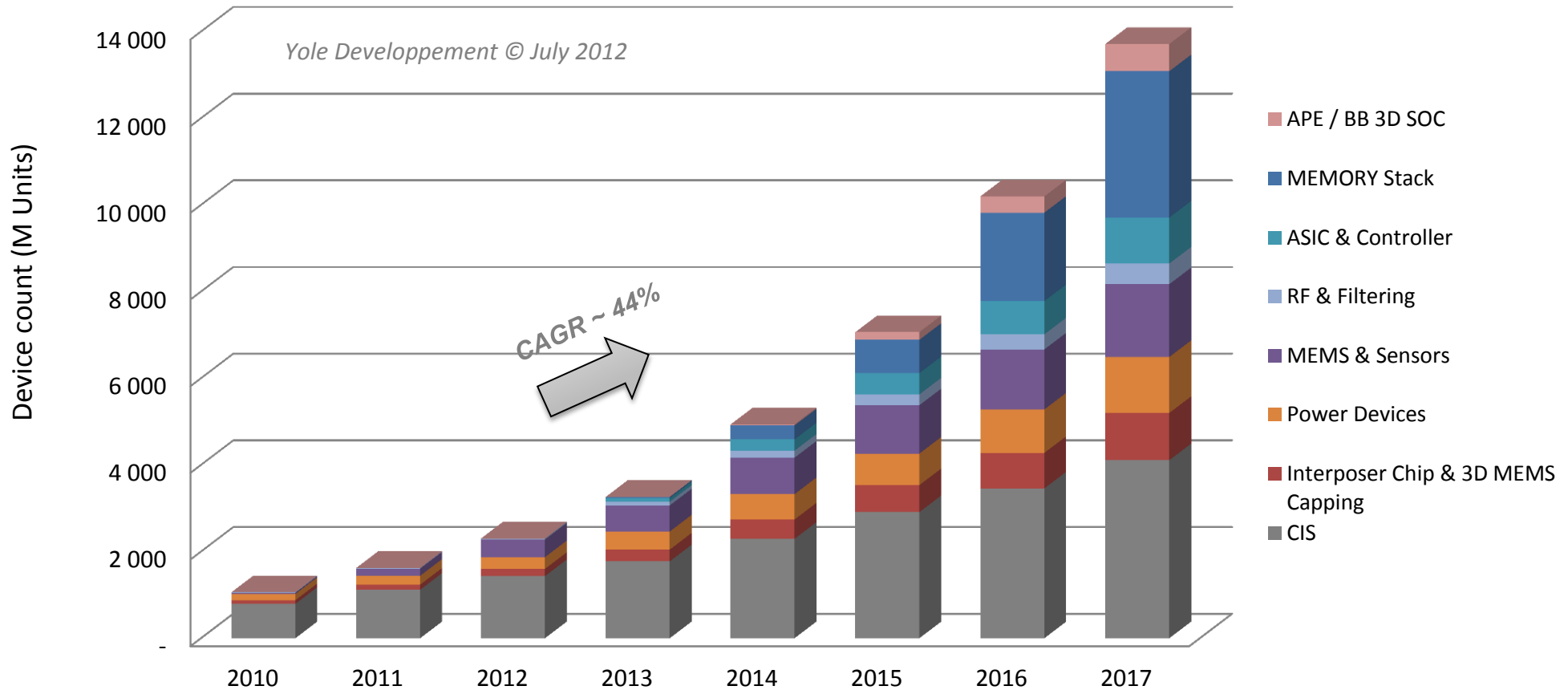
# Global 3D TSV Unit Forecast in Mobile Applications

## Breakdown by IC type (Munits)



### Global 3D TSV Unit Forecast in Mobile Applications

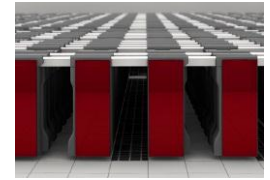
#### Breakdown by IC type (Munits)



- Mobile phones were early adopters of 3D with CIS
- Memory stacked in 3D and CIS is expected to be the top 3D-IC used in mobile applications in 2017, followed by MEMS, power devices and Interposer chips (capping)

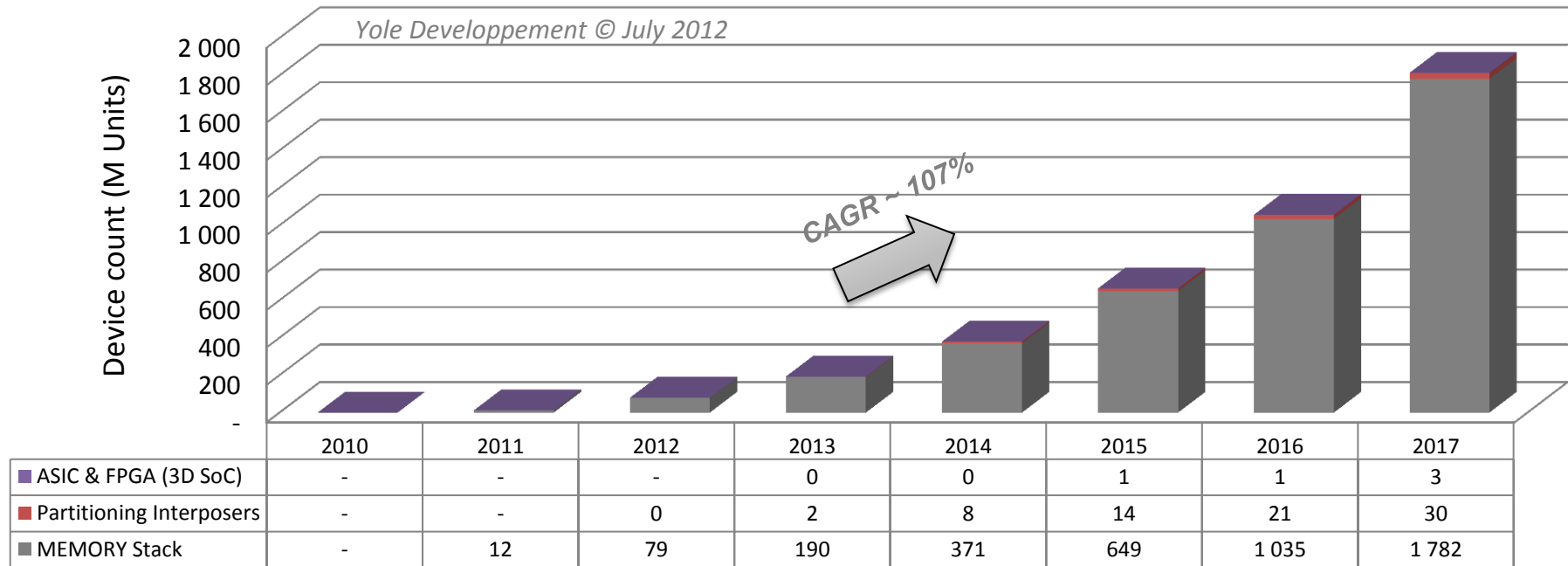
# Global 3D TSV Unit Forecast in Industrial Applications

## Breakdown by IC type (Munits)



### Global 3D TSV Unit Forecast in Industrial Applications

#### Breakdown by IC type (Munits)



- **High-end applications will grow the fastest, at a ~107% CAGR in the 2010-2017 time frame, and will drive initial demand for**
  - Networking memories stacked in 3D
  - FPGAs & high-end ASICs using a system partitioning approach with 2.5D Interposers



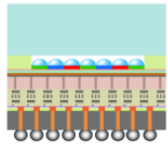
# 3D IC & TSV

## Application Focus

# 3D TSV Application Segmentation

## 3D TSV Applications

### Imaging



WLP CIS

BSI CIS

3D  
integrated  
CIS

Wafer level  
auto-focus

### MEMS & Sensors



Gyros

Acceleros

Pressure sensors

Si-micro

FBAR filters

Oscillators

μProbes

μFluidic / IJ

μValves

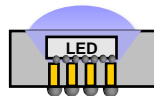
Fingerprint  
sensors

IR-bolometer

Opto (laser, VCSEL)

Micro-mirrors

### HB-LED



Mobile μ-Flash

Automotive

Projection engine

General Lighting

### RF, Power, Analog & Mixed Signal



PA

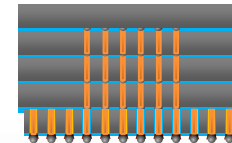
MOSFET

IGBT

IPD

DC-DC  
converters

### Stacked memories

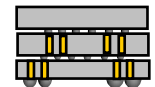


Stacked DRAM

StackedNAND  
Flash

StackedNOR /  
PCRAM

### Logic 3D- SiP/SoC



#### 3D SiP

Wide IO BB

CPU / GPU

FPGA

High. Perf ASICs

#### 3D SoC

Baseband / DSP

MCU / Processors

Touchscreen  
controller

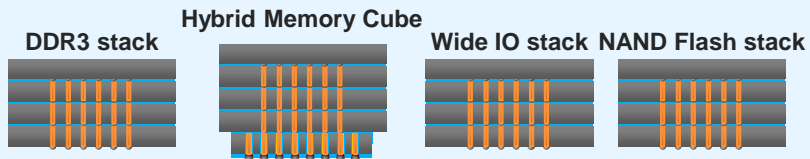
Low-end ASICs

PMIC

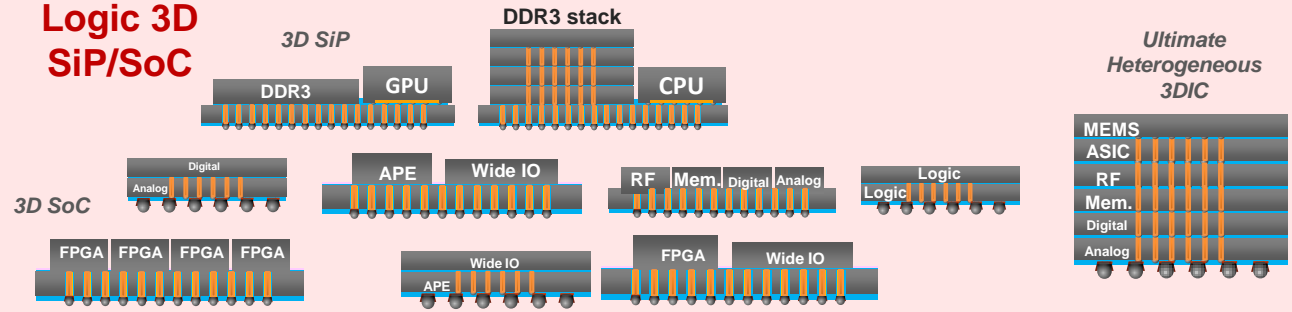
# Global 3DIC & TSV roadmap



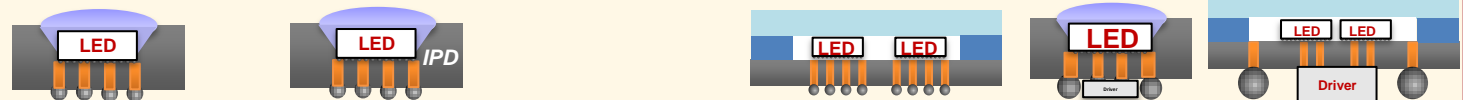
## Stacked Memories



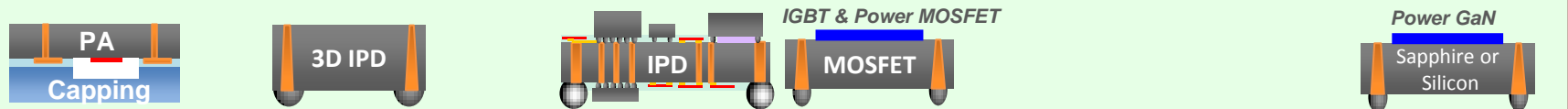
## Logic 3D SiP/SoC



## HB-LED modules



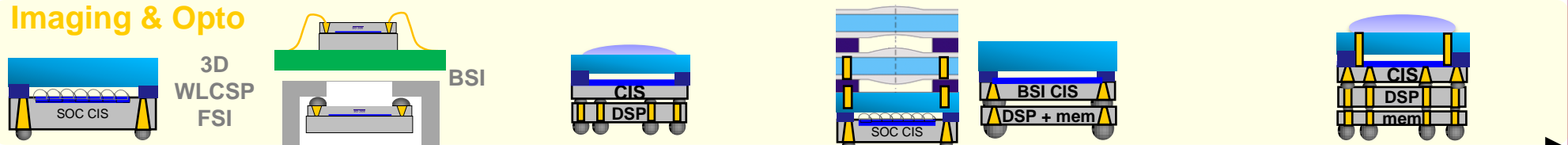
## Power, Analog & RF



## MEMS & Sensors



## Imaging & Opto



< 2009  
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2009

2010

2011

2012

2013

2014

2015

2016

2017

2018

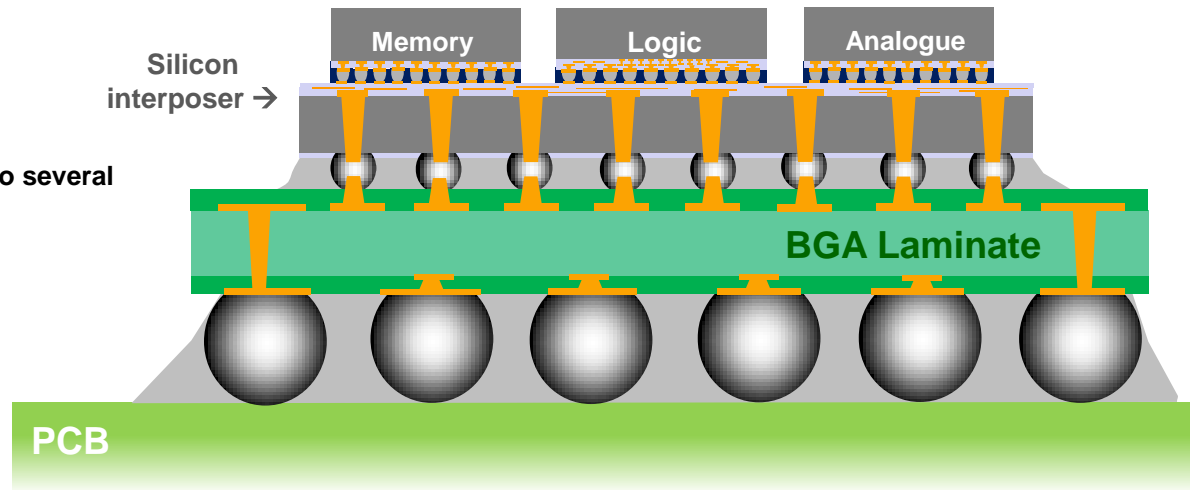
2019

OLE  
ppement

# » System-Partitioning » Interposers

## Definition and drivers

- « System-partitioning » Interposers enable the integration of at least one logic IC with one or several memory ICs, and possible even mixed signal or analog ICs
- They will progressively replace monolithic SoC, or SiP
- Adoption of « system-partitioning » Interposers is driven by
  - Performance
    - Electrical performance is enhanced by placing the various ICs close to one another and by interconnecting them with very high-density and large IO buses, thus enabling high bandwidth between the neighboring ICs on the interposer
    - From a thermal standpoint, 2.5D integration enables similar benefits to those of 3D integration, without the thermal drawbacks of overheating of 3D integration
    - In addition, « system-partitioning » Interposers can act as heat spreaders across the package surface area
  - Cost
    - Each stacked circuit is built using a specific technology tailored to its function (memory, logic, etc.)
  - Yield
    - Some large logic chips can be cut down into several circuits with higher front-end manufacturing yields
- Lead applications for « system-partitioning » are GPUs, FPGAs, large ASICs and APE+memory for tablets
- « System-partitioning » Interposers are generally large (exceeding 20x20mm<sup>2</sup>)

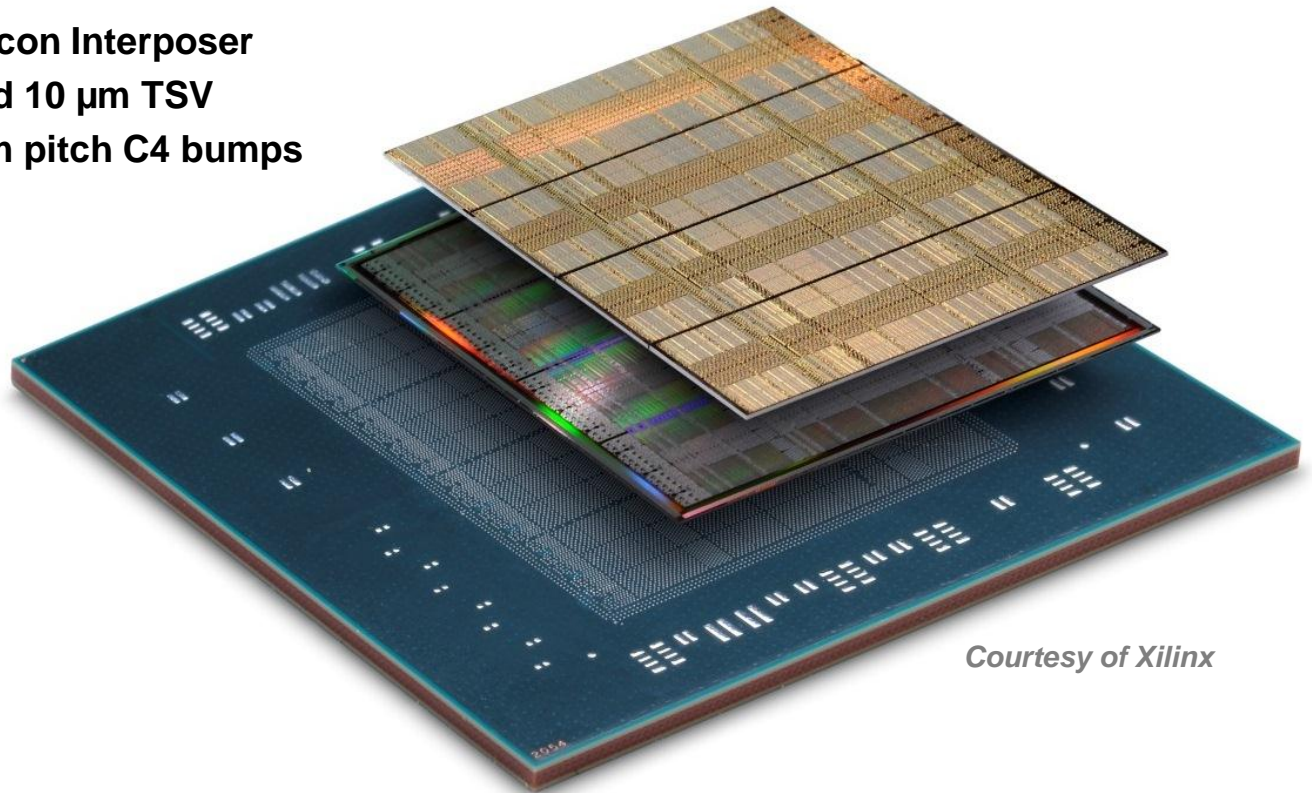


# Interposers for FPGA

## Focus on Xilinx Virtex 7 HT



- Last fall, Xilinx announced a single-layer, multi-chip silicon interposer for its 28nm 7 series FPGAs
- Key features
  - Two million logic cells for a high level of computational performance ,and high bandwidth
  - Four slice processed in 28 nm
  - 25 x 31mm, 100  $\mu$ m thick silicon Interposer
  - 45  $\mu$ m pitch microbumps and 10  $\mu$ m TSV
  - 35 x 35 mm BGA with 180  $\mu$ m pitch C4 bumps
- Even if the infrastructure had been ready for full 3D stacking, the 2.5D Interposer would still have been the right choice for FPGAs since the “10,000 routing connections” would have used up valuable chip area, making the chip slices larger and more costly than they are now
- Virtex 7 HT will consist of three FPGA slices and two 28 gbps SerDes chips on an Interposer capable of operating at 2.8 Tb/sec!

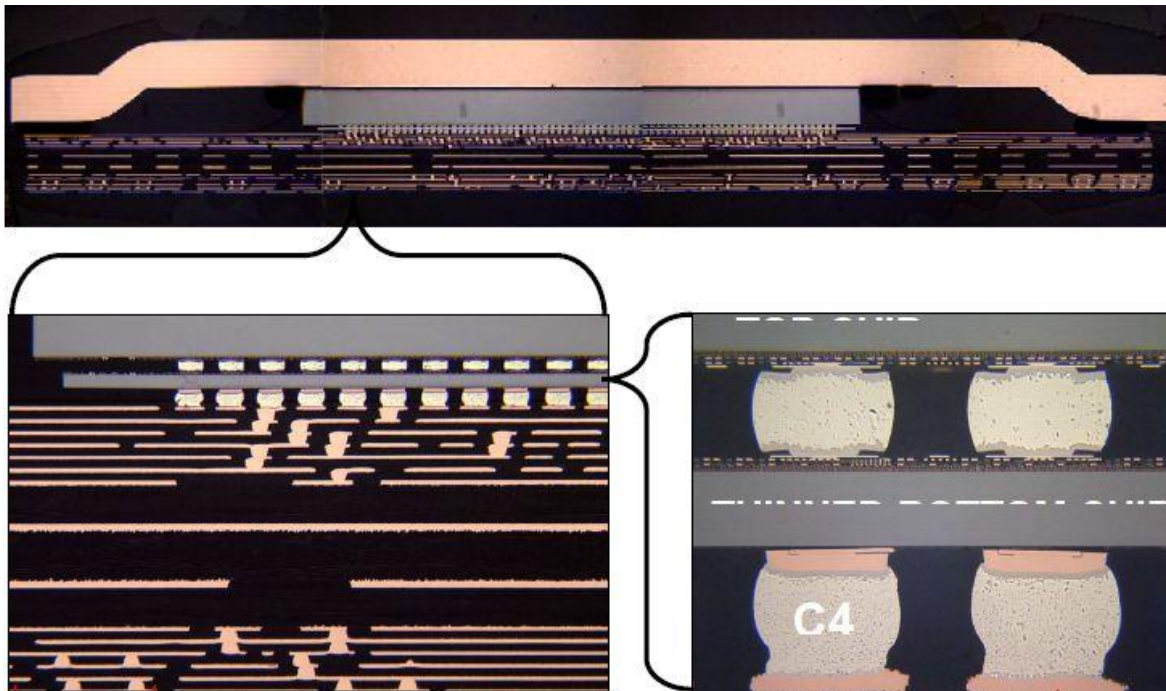


*Courtesy of Xilinx*

Source: Yole Développement & Phil Garrou for iMicronews

# Interposers for Large CPUs and GPUs

- **Limitation/Bottleneck in conventional 2D architecture**
  - Beyond eight cores, processors will lose performance benefits in a 2D configuration. This is a fundamental bottleneck that IBM and Intel are working on
    - 2D SoC partitioning and use of 2.5D Interposers will be soon be mandatory for increasing the performance of high-performance computers!
- **Power 8 by IBM will be based on 2.5D Interposers**
- **Haswel, Intel GPU on 2.5D Interposers for laptops, with lots of on-board memory and an ultra-large data bus**



Cross-section pictures of an IBM 3D stacked module demonstrator with TSVs in the thinner die  
(courtesy of Chipworks)

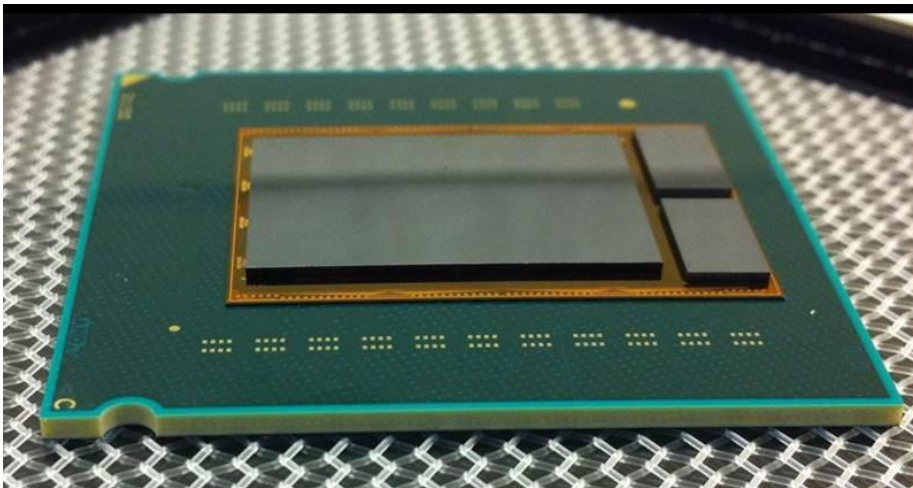


IBM Power 7+: four 32nm CMOS multi-core CPU dies are placed side by side on a silicon Interposer. (Courtesy of SemiAccurate.com)

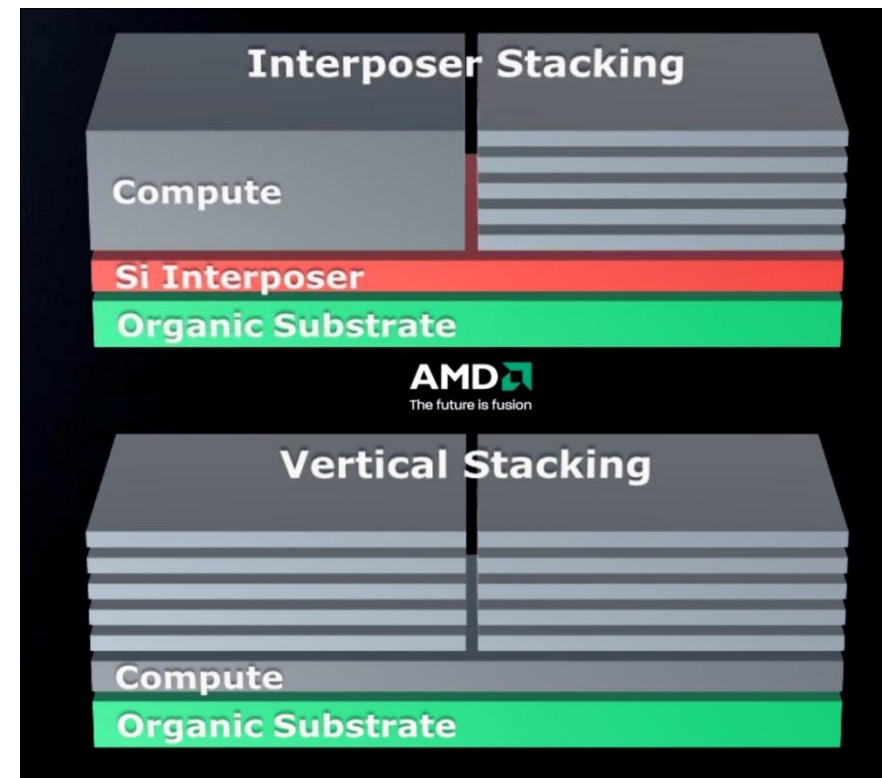


# GPU for Gaming

- Sony's PS4 (2013) will have its GPU and memory stacked on a 2.5D Silicon Interposer with a 512-wide data bus. This will likely be an AMD chip
- Future gaming platforms will offer 3D imagery, which requires fast & high bandwidth computing power
- 2.5D is unanimously praised as the solution for this purpose
- **“GPU-RAM bandwidth is the key factor for rendering performance” – Sept 2011, Teiji Yutaka , SVP Technology Platform, Sony Computer Entertainment**

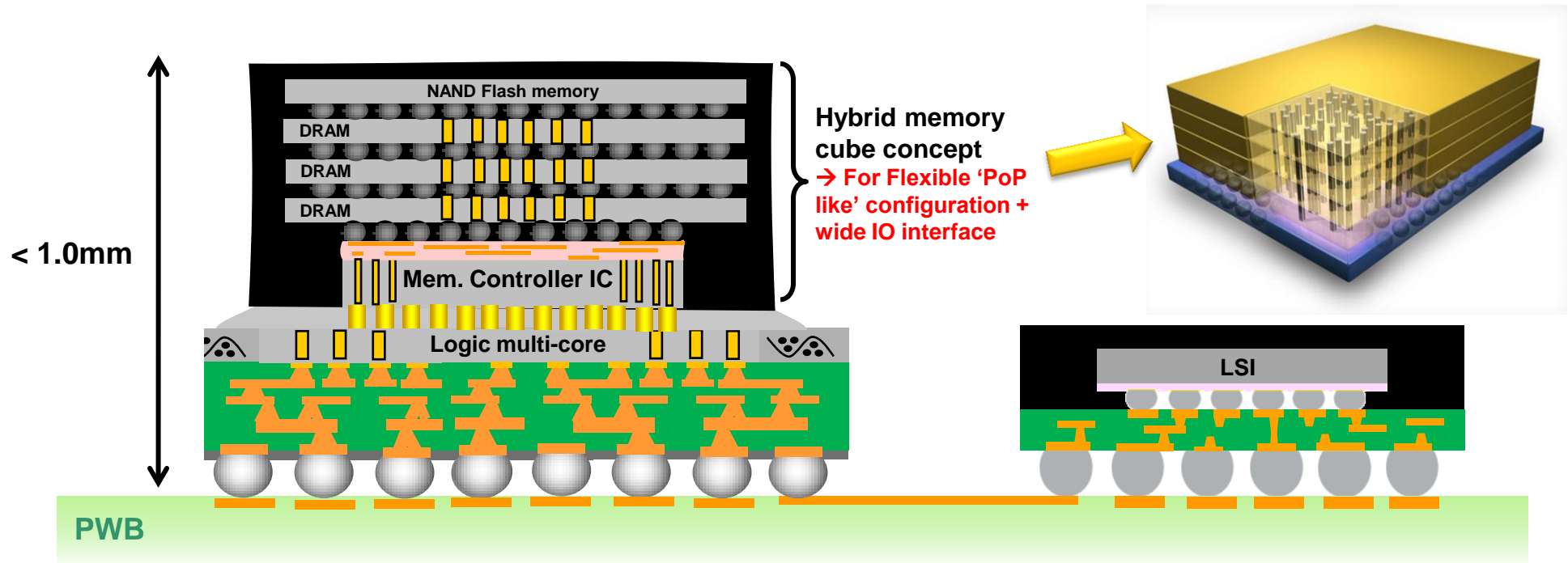


*An Interposer module for (Yole's assumption) an AMD GPU demonstrator, Courtesy of Global Foundries, 2012*





# Micron/Samsung/IBM « HMC » Hybrid Memory Cube Technology for Wide IO Interface in LSI Applications



- Micron/Samsung/IBM recently announced a partnership in 3DIC for Wide IO interface dedicated to high-performance LSI applications (networking & storage ASICs, FPGA, etc.) The technology will enable
  - Reduced cost of memory and logic SOC designs, thanks to integration of memory management functionalities within the memory controller IC manufactured by IBM (US)
  - **Highly flexible “memory to logic” integration** with the capability to scale with different memory/logic technology nodes and interfaces
  - Easier **testability** of memory stack prior to assembly to logic package

# Conclusions & Perspectives



# Main Conclusions and Perspectives

- **3DIC technology is considered today as a new paradigm for the future of the semiconductor industry!**
  - 3DIC will enable several more decades of chip evolution at ever lower cost, higher performance and smaller-size features
- **3D stacked DRAM and 3D Logic SOC applications are expected to be the biggest drivers for the volume adoption of 3DIC technology in the next five years, followed by CMOS image sensors, power devices and MEMS**
  - Today, the market is driven by high-end applications using 2.5D partitioning Interposers
  - Large-die FPGAs and ASICs are on the way to being commercialized for industrial applications, and are also expected to grow in the near future in the gaming and smart TV markets
- **2013 will likely be the key turning point for the first true implementation of 3DIC technology in significant volume, driven by the commercialization of hybrid memory cubes**
- **In terms of value, the 3D TSV market will reach \$40B in 2017, growing more than 10 times faster than the global semiconductor industry!**
  - Looking closer at the Interposer industry -- as of 2017, Yole expects 2.5D Interposer revenues to attain 14% of the packaging substrate market value
  - 3D WLCSP is the preferred solution today for the efficient assembly of small-size optoelectronic chips like CMOS image sensors. It is also the most mature 3D TSV platform at the moment, as we estimate the market to be ~ \$270M in 2011 for the “middle-end” processing factories serving this specific market